Ultra-Tiny, 16-Bit ΔΣ ADCs with 10ppm/°C Max Precision Reference

FEATURES

- **16-Bit Resolution, No Missing Codes**
- **Internal Reference, High Accuracy 10ppm/°C (Max)**
- **Single-Ended (LTC2460) or Differential (LTC2462)**
- **2LSB Offset Error**
- **0.01% Gain Error**
- **60 Conversions Per Second**
- Single Conversion Settling Time for Multiplexed Applications
- Single-Cycle Operation with Auto Shutdown
- 1.5mA Supply Current
- 2µA (Max) Sleep Current
- Internal Oscillator—No External Components Required
- SPI Interface
- Ultra-Tiny 12-Lead 3mm × 3mm DFN and MSOP Packages

APPLICATIONS

- System Monitoring
- Environmental Monitoring
- Direct Temperature Measurements
- Instrumentation
- Industrial Process Control
- Data Acquisition
- Embedded ADC Upgrades

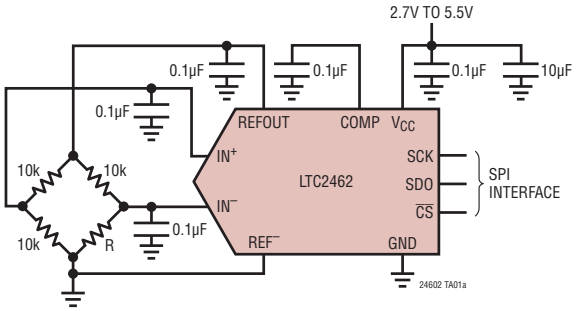
DESCRIPTION

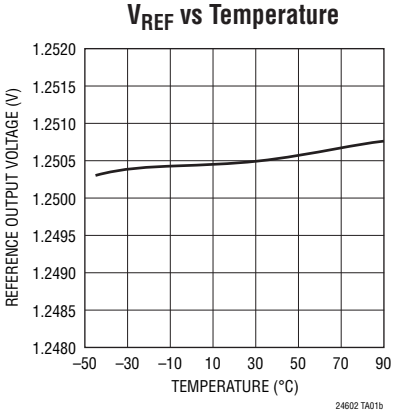
The LTC®2460/LTC2462 are ultra tiny, 16-Bit analog-to-digital converters with an integrated precision reference. They use a single 2.7V to 5.5V supply and communicate through an SPI Interface. The LTC2460 is single-ended with a 0V to V_{REF} input range and the LTC2462 is differential with a $\pm V_{REF}$ input range. Both ADC's include a 1.25V integrated reference with 2ppm/°C drift performance and 0.1% initial accuracy. The converters are available in a 12-pin DFN 3mm × 3mm package or an MSOP-12 package. They include an integrated oscillator and perform conversions with no latency for multiplexed applications. The LTC2460/LTC2462 include a proprietary input sampling scheme that reduces the average input current several orders of magnitude when compared to conventional delta sigma converters.

Following a single conversion, the LTC2460/LTC2462 automatically power down the converter and can also be configured to power down the reference. When both the ADC and reference are powered down, the supply current is reduced to 200nA.

The LTC2460/LTC2462 can sample at 60 conversions per second, and due to the very large oversampling ratio, have extremely relaxed antialiasing requirements. Both include continuous internal offset and fullscale calibration algorithms which are transparent to the user, ensuring accuracy over time and the operating temperature range.

TYPICAL APPLICATION





ABSOLUTE MAXIMUM RATINGS

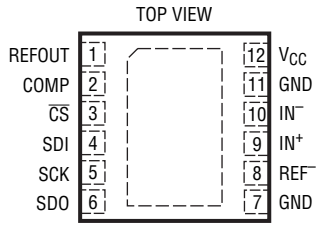
(Notes 1, 2)

Supply Voltage (V_{CC}) ..... –0.3V to 6V
Analog Input Voltage
(IN^+, IN^-, IN, REF^-,
COMP, REFOUT) .....–0.3V to (V_{CC} + 0.3V)
Digital Voltage
(V_{SDI}, V_{SDO}, V_{SCK}, $V_{\overline{CS}}$) .....–0.3V to (V_{CC} + 0.3V)

Storage Temperature Range ..... –65°C to 150°C
Operating Temperature Range
LTC2460C/LTC2462C..... 0°C to 70°C
LTC2460I/LTC2462I .....–40°C to 85°C

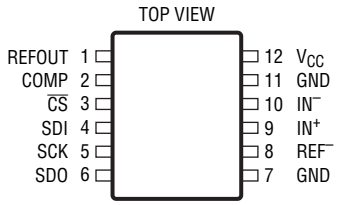
PIN CONFIGURATION

LTC2462



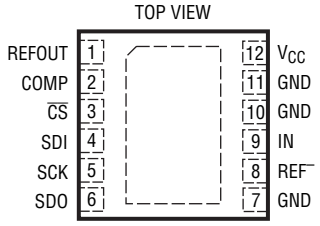
DD PACKAGE
12-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) PCB GROUND CONNECTION OPTIONAL

LTC2462



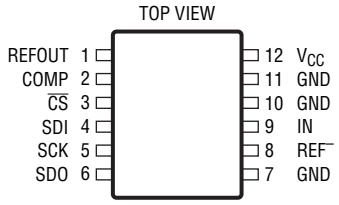
MS PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 120°C/W

LTC2460



DD PACKAGE
12-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) PCB GROUND CONNECTION OPTIONAL

LTC2460



MS PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 120°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2460CDD#PBF	LTC2460CDD#TRPBF	LFDQ	12-Lead Plastic (3mm × 3mm) DFN	0°C to 70°C
LTC2460IDD#PBF	LTC2460IDD#TRPBF	LFDQ	12-Lead Plastic (3mm × 3mm) DFN	–40°C to 85°C
LTC2460CMS#PBF	LTC2460CMS#TRPBF	2460	12-Lead Plastic MSOP-12	0°C to 70°C
LTC2460IMS#PBF	LTC2460IMS#TRPBF	2460	12-Lead Plastic MSOP-12	–40°C to 85°C
LTC2462CDD#PBF	LTC2462CDD#TRPBF	LDXM	12-Lead Plastic (3mm × 3mm) DFN	0°C to 70°C
LTC2462IDD#PBF	LTC2462IDD#TRPBF	LDXM	12-Lead Plastic (3mm × 3mm) DFN	–40°C to 85°C
LTC2462CMS#PBF	LTC2462CMS#TRPBF	2462	12-Lead Plastic MSOP-12	0°C to 70°C
LTC2462IMS#PBF	LTC2462IMS#TRPBF	2462	12-Lead Plastic MSOP-12	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	(Note 3)	●	16			Bits
Integral Nonlinearity	(Note 4)	●		1	10	LSB
Offset Error		●		2	15	LSB
Offset Error Drift				0.02		LSB/°C
Gain Error	Includes Contributions of ADC and Internal Reference	●		±0.01	±0.25	% of FS
Gain Error Drift	Includes Contributions of ADC and Internal Reference C-Grade I-Grade	 ● ●		 ±2 ±5	 ±10	 ppm/°C ppm/°C
Transition Noise				2.2		μV_{RMS}
Power Supply Rejection DC				80		dB

ANALOG INPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}^+	Positive Input Voltage Range	LTC2462	●	0		V_{REF}	V
V_{IN}^-	Negative Input Voltage Range	LTC2462	●	0		V_{REF}	V
V_{IN}	Input Voltage Range	LTC2460	●	0		V_{REF}	V
V_{OR}^+, V_{UR}^+	Overrange/Underrange Voltage, IN^+	V_{IN}^- = 0.625V (See Figure 3)			8		LSB
V_{OR}^-, V_{UR}^-	Overrange/Underrange Voltage, IN–	V_{IN}^+ = 0.625V (See Figure 3)			8		LSB
C_{IN}	IN^+, IN^-, IN Sampling Capacitance				0.35		pF
$I_{DC\_LEAK(IN^+, IN^-, IN)}$	IN^+, IN^- DC Leakage Current (LTC2462) IN DC Leakage Current (LTC2460)	V_{IN} = GND (Note 8) V_{IN} = V_{CC} (Note 8)	● ●	–10 –10	1 1	10 10	nA nA
$I_{DC\_LEAK(IN^-)}$	IN^- DC Leakage Current	V_{IN} = GND (Note 8) V_{IN} = V_{CC} (Note 8)	● ●	–10 –10	1 1	10 10	nA nA
I_{CONV}	Input Sampling Current (Note 5)				50		nA
V_{REF}	Reference Output Voltage		●	1.247	1.25	1.253	V
	Reference Voltage Coefficient	(Note 11) C-Grade I-Grade	 ● ●		 ±2 ±5	 ±10	 ppm/°C ppm/°C
	Reference Line Regulation	2.7V ≤ V_{CC} ≤ 5.5V			–90		dB
	Reference Short Circuit Current	V_{CC} = 5.5, Forcing Output to GND	●			35	mA
	COMP Pin Short Circuit Current	V_{CC} = 5.5, Forcing Output to GND	●			200	µA
	Reference Load Regulation	2.7V ≤ V_{CC} ≤ 5.5V, I_{OUT} = 100µA Sourcing			3.5		mV/mA
	Reference Output Noise Density	C_{COMP}= 0.1µF, C_{REFOUT} = 0.1µF, At f = 1kHz			30		nV/√Hz

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current Conversion Nap Sleep		 ● ● ●		 1.5 800 0.2	 2.5 1500 2	 mA µA µA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	V_{CC} – 0.3			V
V_{IL}	Low Level Input Voltage		●			0.3	V
I_{IN}	Digital Input Current		●	–10		10	µA
C_{IN}	Digital Input Capacitance				10		pF
V_{OH}	High Level Output Voltage	I_O = –800µA	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage	I_O = 1.6mA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage Current		●	–10		10	µA

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{CONV}	Conversion Time		●	13	16.6	23	ms
f_{SCK}	SCK Frequency Range		●			2	MHz
t_{lSCK}	SCK Low Period		●	250			ns
t_{hSCK}	SCK High Period		●	250			ns
t_1	$\overline{CS}$ Falling Edge to SDO Low Z	(Notes 7, 8)	●	0		100	ns
t_2	$\overline{CS}$ Rising Edge to SDO High Z	(Notes 7, 8)	●	0		100	ns
t_3	$\overline{CS}$ Falling Edge to SCK Falling Edge		●	100			ns
t_{KQ}	SCK Falling Edge to SDO Valid	(Note 7)	●	0		100	ns
t_4	SDI Setup Before SCK↑	(Note 3)	●	100			ns
t_5	SDI Hold After SCK↑	(Note 3)	●	100			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. All voltage values are with respect to GND. V_{CC} = 2.7V to 5.5V unless otherwise specified.

$V_{REFCM} = V_{REF}/2$, FS = V_{REF}

$V_{IN} = V_{IN}^+ – V_{IN}^–$, $–V_{REF} \le V_{IN} \le V_{REF}$; $V_{INCM} = (V_{IN}^+ + V_{IN}^–)/2$.

Note 3. Guaranteed by design, not subject to test.

Note 4. Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. Guaranteed by design and test correlation.

Note 5: $\overline{CS}$ = V_{CC}. A positive current is flowing into the DUT pin.

Note 6: SCK = V_{CC} or GND. SDO is high impedance.

Note 7: See Figure 4.

Note 8: See Figure 5.

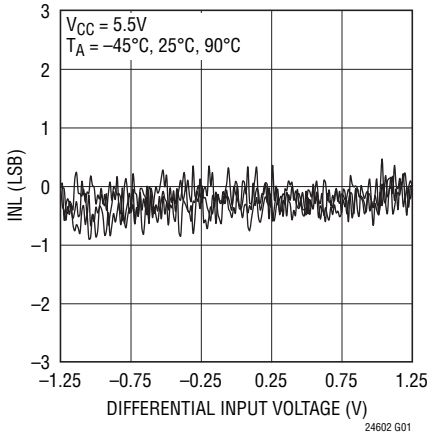
Note 9: Input sampling current is the average input current drawn from the input sampling network while the LTC2460/LTC2462 is actively sampling the input.

Note 10: A positive current is flowing into the DUT pin.

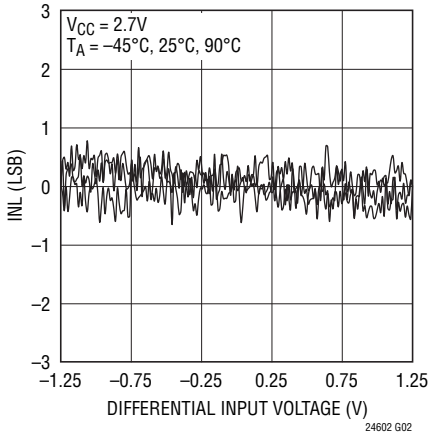
Note 11: Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

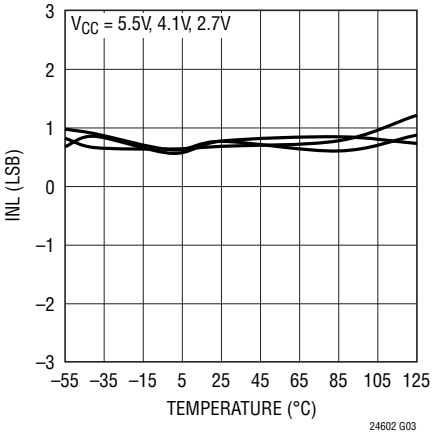
Integral Nonlinearity



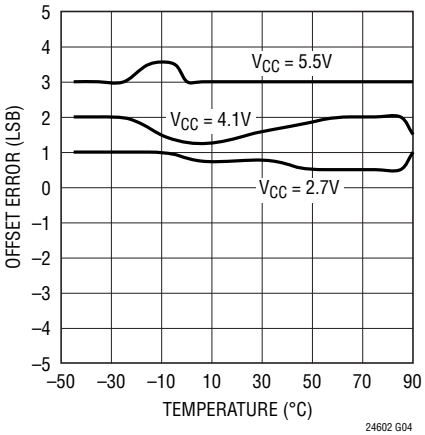
Integral Nonlinearity



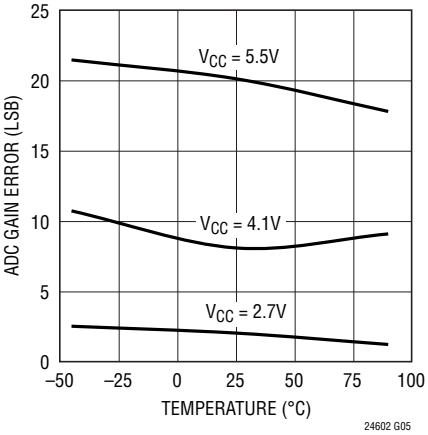
Maximum INL vs Temperature



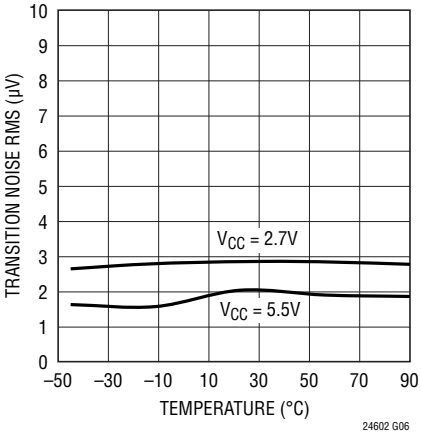
Offset Error vs Temperature



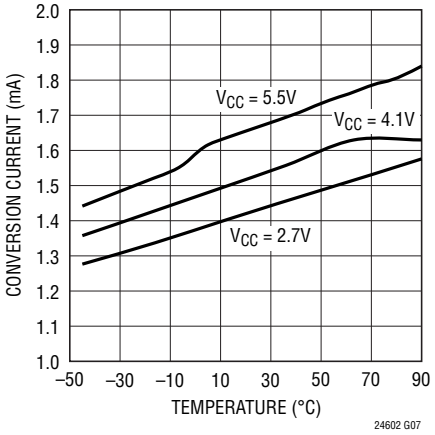
ADC Gain Error vs Temperature



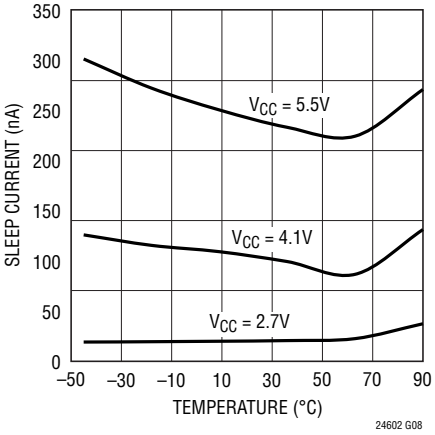
Transition Noise vs Temperature



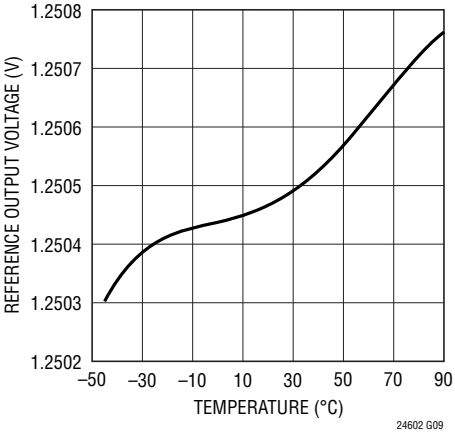
Conversion Mode Power Supply Current vs Temperature



Sleep Mode Power Supply Current vs Temperature

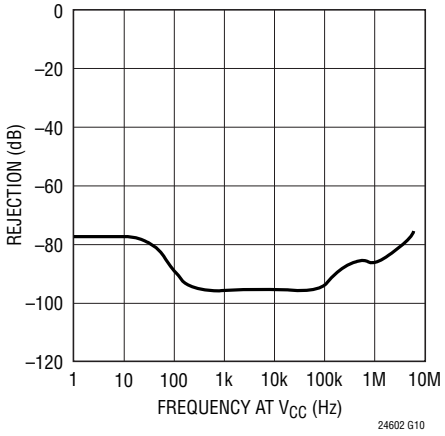


V_{REF} vs Temperature

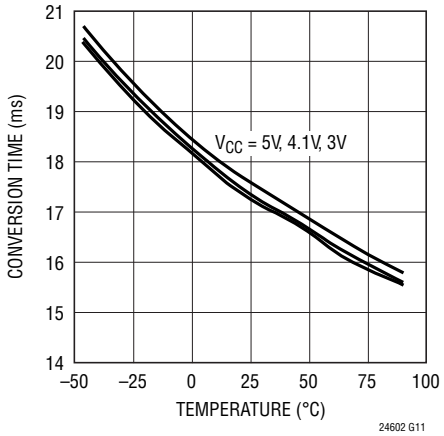


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

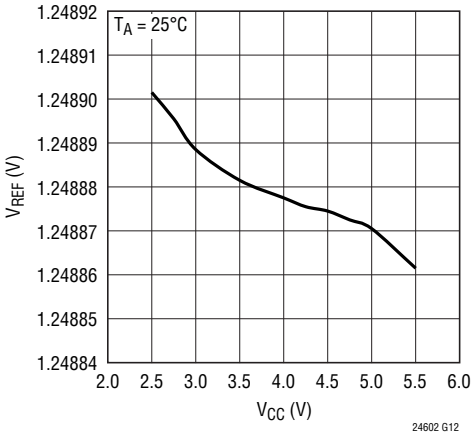
Power Supply Rejection vs Frequency at V_{CC}



Conversion Time vs Temperature



V_{REF} vs V_{CC}



PIN FUNCTIONS

REFOUT (Pin 1): Reference Output Pin. Nominally 1.25V, this voltage sets the fullscale input range of the ADC. For noise and reference stability connect to a 0.1µF capacitor tied to GND. This capacitor value must be less than or equal to the capacitor tied to the reference compensation pin (COMP). REFOUT cannot be overdriven by an external reference. For applications that require an input range greater than 0V to 1.25V, please refer to the LTC2450/LTC2452.

COMP (Pin 2): Internal Reference Compensation Pin. For low noise and reference stability, tie a 0.1µF capacitor to GND.

$\overline{CS}$ (Pin 3): Chip Select (Active LOW) Digital Input. A LOW on this pin enables the SDO output. A HIGH on this pin places the SDO output pin in a high impedance state and any inputs on SDI and SCK will be ignored.

SDI (Pin 4): Serial Data Input Pin. This pin is used to program the sleep mode and 30Hz/60Hz output rate (LTC2460).

SCK (Pin 5): Serial Clock Input. SCK synchronizes the serial data input/output. Once the conversion is complete, a new data bit is produced at the SDO pin following each SCK falling edge. Data is shifted into the SDI pin on each rising edge of SCK.

SDO (Pin 6): Three-State Serial Data Output. SDO is used for serial data output during the DATA INPUT/OUTPUT state and can be used to monitor the conversion status.

GND (Pins 7, 11): Ground. Connect directly to the ground plane through a low impedance connection.

REF^- (Pin 8): Negative Reference Input to the ADC. The voltage on this pin sets the zero input to the ADC. This pin should tie directly to ground or the ground sense of the input sensor.

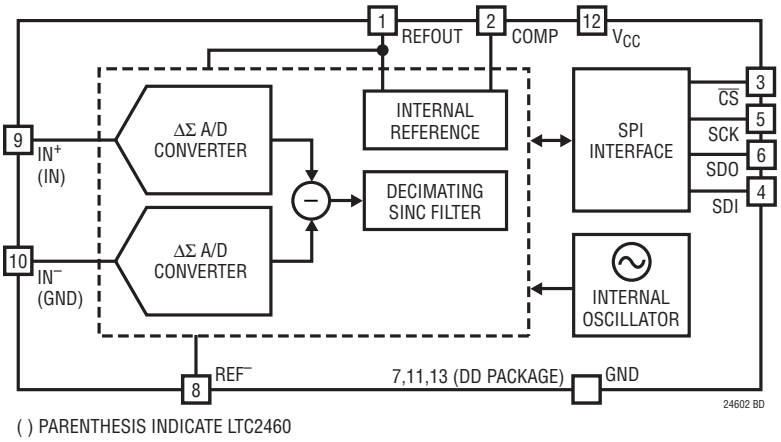
IN^+ (LTC2462), IN (LTC2460) (Pin 9): Positive input voltage for the LTC2462 differential device. ADC input for the LTC2460 single-ended device.

IN^- (LTC2462), GND (LTC2460) (Pin 10): Negative input voltage for the LTC2462 differential device. GND for the LTC2460 single-ended device.

V_{CC} (Pin 12): Positive Supply Voltage. Bypass to GND with a 10µF capacitor in parallel with a low-series-inductance 0.1µF capacitor located as close to the device as possible.

Exposed Pad (Pin 13 – DFN Package): Ground. Connect directly to the ground plane through a low impedance connection.

BLOCK DIAGRAM



( ) PARENTHESIS INDICATE LTC2460

Figure 1. Functional Block Diagram

APPLICATIONS INFORMATION

CONVERTER OPERATION

Converter Operation Cycle

The LTC2460/LTC2462 are low power, delta sigma, analog to digital converters with a simple SPI interface (see Figure 1). The LTC2462 has a fully differential input while the LTC2460 is single-ended. Both are pin and software compatible. Their operation is composed of three distinct states: CONVERT, SLEEP/NAP, and DATA INPUT/OUTPUT. The operation begins with the CONVERT state (see Figure 2). Once the conversion is finished, the converter automatically powers down (NAP) or under user control, both the converter and reference are powered down (SLEEP). The conversion result is held in a static register while the device is in this state. The cycle concludes with the DATA INPUT/OUTPUT state. Once all 16-bits are read or an abort is initiated the device begins a new conversion.

The CONVERT state duration is determined by the LTC2460/LTC2462 conversion time (nominally 16.6 milliseconds). Once started, this operation can not be aborted except by a low power supply condition (V_{CC} < 2.1V) which generates an internal power-on reset signal.

After the completion of a conversion, the LTC2460/LTC2462 enters the SLEEP/NAP state and remains there until the chip select is LOW ($\overline{CS}$ = LOW). Following this condition, the ADC transitions into the DATA INPUT/OUTPUT state.

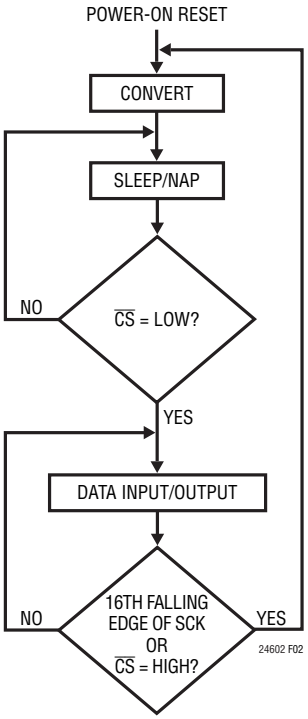


Figure 2. LTC2460/LTC2462 State Transition Diagram

While in the SLEEP/NAP state, when chip select input is HIGH ($\overline{CS}$ = HIGH), the LTC2460/LTC2462's converters are powered down. This reduces the supply current by approximately 50%. While in the Nap state the reference remains powered up. In order to power down the reference in addition to the converter, the user can select the SLEEP

APPLICATIONS INFORMATION

mode during the DATA INPUT/OUTPUT state. Once the next conversion is complete, the SLEEP state is entered and power is reduced to less than 2µA. The reference is powered up once $\overline{CS}$ is brought low. The reference startup time is 12ms (if the reference and compensation capacitor values are both 0.1µF).

Upon entering the DATA INPUT/OUTPUT state, SDO outputs the sign (D15) of the conversion result. During this state, the ADC shifts the conversion result serially through the SDO output pin under the control of the SCK input pin. There is no latency in generating this data and the result corresponds to the last completed conversion. A new bit of data appears at the SDO pin following each falling edge detected at the SCK input pin and appears from MSB to LSB. The user can reliably latch this data on every rising edge of the external serial clock signal driving the SCK pin.

During the DATA INPUT/OUTPUT state, the LTC2460/LTC2462 can be programmed to SLEEP or NAP (default) following the next conversion cycle. Data is shifted into the device through the SDI pin on the rising edge of SCK. The input word is 4 bits. If the first bit EN1 = 1 and the second bit EN2 = 0 the device is enabled for programming. The following two bits (SPD and SLP) will be written into the device. SPD (only used for the LTC2460) to select the 60Hz output rate, no offset calibration mode (SPD = 0, default). Set SPD = 1 for 30Hz mode with offset calibration. SPD is ignored for the LTC2462. The next bit (SLP) enables the sleep or nap mode. If SLP = 0 (default) the reference remains powered up at the end of the next conversion cycle. If SLP = 1, the reference powers down following the next conversion cycle. The remaining 12 SDI input bits are ignored (don't care).

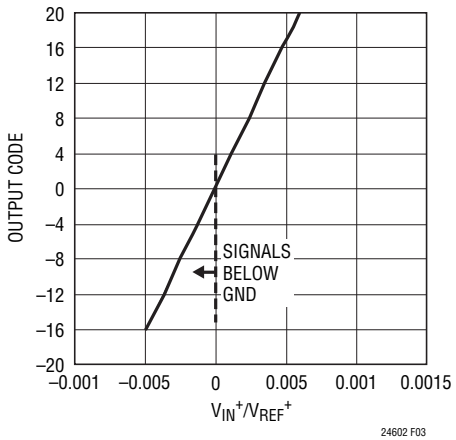


Figure 3. Output Code vs V_{IN}^+ with V_{IN}^- = 0 (LTC2462)

SDI may also be tied directly to GND or V_{DD} in order to simplify the user interface. In the case of the LTC2460, the 60Hz output rate is selected if SDI is tied low and the 30Hz output rate is selected if SDI is tied to V_{DD}. The LTC2462 output rate is always 60Hz independent of SDI or SPD. The reference sleep mode is disabled for both the LTC2460 and LTC2462 if SDI is tied to GND or V_{DD}.

The DATA INPUT/OUTPUT state concludes in one of two different ways. First, the DATA INPUT/OUTPUT state operation is completed once all 16 data bits have been shifted out and the clock then goes low. This corresponds to the 16th falling edge of SCK. Second, the DATA INPUT/OUTPUT state can be aborted at any time by a LOW-to-HIGH transition on the $\overline{CS}$ input. Following either one of these two actions, the LTC2460/LTC2462 will enter the CONVERT state and initiate a new conversion cycle.

Power-Up Sequence

When the power supply voltage (V_{CC}) applied to the converter is below approximately 2.1V, the ADC performs a power-on reset. This feature guarantees the integrity of the conversion result.

When V_{CC} rises above this critical threshold, the converter generates an internal power-on reset (POR) signal for approximately 0.5ms. The POR signal clears all internal registers. Following the POR signal, the LTC2460/LTC2462 start a conversion cycle and follow the succession of states shown in Figure 2. The reference startup time following a POR is 12ms (C_{COMP} = C_{REFOUT} = 0.1µF). The first conversion following powerup will be invalid since the reference voltage has not completely settled. The first conversion following power up can be discarded using the data abort command or simply read and ignored. The following conversions are accurate to the device specifications.

Ease of Use

The LTC2460/LTC2462 data output has no latency, filter settling delay or redundant results associated with the conversion cycle. There is a one-to-one correspondence

APPLICATIONS INFORMATION

between the conversion and the output data. Therefore, multiplexing multiple analog input voltages requires no special actions.

The LTC2460/LTC2462 perform offset calibrations every conversion. This calibration is transparent to the user and has no effect upon the cyclic operation described previously. The advantage of continuous calibration is stability of the ADC performance with respect to time and temperature.

The LTC2460/LTC2462 include a proprietary input sampling scheme that reduces the average input current by several orders of magnitude when compared to traditional delta-sigma architectures. This allows external filter networks to interface directly to the LTC2460/LTC2462. Since the average input sampling current is 50nA, an external RC lowpass filter using 1kΩ and 0.1µF results in <1LSB additional error. Additionally, there is negligible leakage current between IN^+ and IN^-.

Input Voltage Range (LTC2460)

Ignoring offset and full-scale errors, the LTC2460 will theoretically output an "all zero" digital result when the input is at ground (a zero scale input) and an "all one" digital result when the input is at V_{REF} (V_{REFOUT} = 1.25V). In an under-range condition, for all input voltages below zero scale, the converter will generate the output code 0. In an over-range condition, for all input voltages greater than V_{REF}, the converter will generate the output code 65535. For applications that require an input range greater than 0V to 1.25V, please refer to the LTC2450.

Input Voltage Range (LTC2462)

As mentioned in the Output Data Format section, the output code is given as 32768 • $(V_{IN}^+ – V_{IN}^-)/V_{REF}$ + 32768. For $(V_{IN}^+ – V_{IN}^-) \geq V_{REF}$, the output code is clamped at 65535 (all ones). For $(V_{IN}^+ – V_{IN}^-) \leq –V_{REF}$, the output code is clamped at 0 (all zeroes).

The LTC2462 includes a proprietary architecture that can, typically, digitize each input up to 8 LSBs above V_{REF} and below GND, if the differential input is within $\pm V_{REF}$. As an example (Figure 3), if the user desires to measure a signal slightly below ground, the user could set V_{IN}^- = GND, and V_{REF} = 1.25V. If V_{IN}^+ = GND, the output code would be approximately 32768. If V_{IN}^+ = GND – 8LSB = –0.305mV, the output code would be approximately 32760. For applications that require an input range greater than ±1.25V, please refer to the LTC2452.

Output Data Format

The LTC2460/LTC2462 generates a 16-bit direct binary encoded result. It is provided as a 16-bit serial stream through the SDO output pin under the control of the SCK input pin (see Figure 4).

The LTC2462 (differential input) output code is given by 32768 • $(V_{IN}^+ – V_{IN}^-)/V_{REF}$ + 32768. The first bit output by the LTC2462, D15, is the MSB, which is 1 for $V_{IN}^+ \geq V_{IN}^-$ and 0 for $V_{IN}^+ < V_{IN}^-$. This bit is followed by successively less significant bits (D14, D13, …) until the LSB is output by the LTC2462, see Table 1.

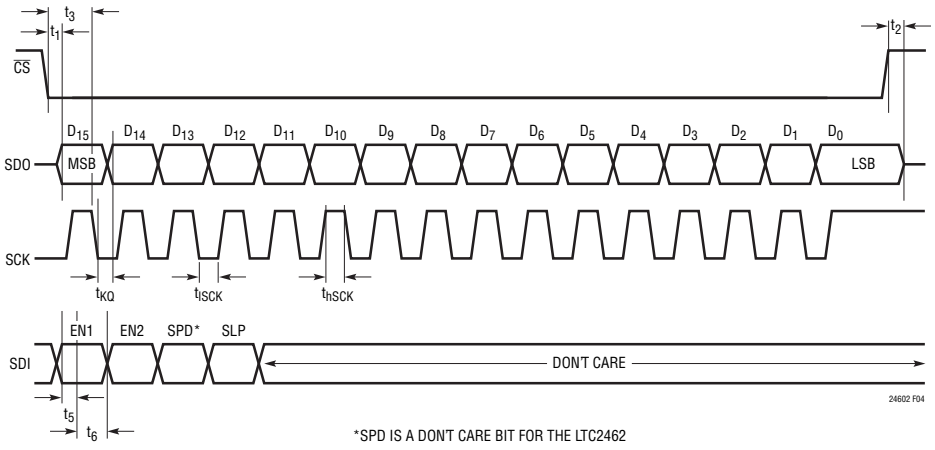


Figure 4. Data Input/Output Timing

APPLICATIONS INFORMATION

Table 1. LTC2460/LTC2462 Output Data Format

SINGLE ENDED INPUT V_{IN} (LTC2460)	DIFFERENTIAL INPUT VOLTAGE $V_{IN}^+ - V_{IN}^-$ (LTC2462)	D15 (MSB)	D14	D13	D12…D2	D1	D0 (LSB)	CORRESPONDING DECIMAL VALUE
≥V_{REF}	≥V_{REF}	1	1	1	1	1	1	65535
V_{REF} – 1LSB	V_{REF} – 1LSB	1	1	1	1	1	0	65534
0.75 • V_{REF}	0.5 • V_{REF}	1	1	0	0	0	0	49152
0.75 • V_{REF} – 1LSB	0.5 • V_{REF} – 1LSB	1	0	1	1	1	1	49151
0.5 • V_{REF}	0	1	0	0	0	0	0	32768
0.5 • V_{REF} – 1LSB	–1LSB	0	1	1	1	1	1	32767
0.25 • V_{REF}	–0.5 • V_{REF}	0	1	0	0	0	0	16384
0.25 • V_{REF} – 1LSB	–0.5 • V_{REF} – 1LSB	0	0	1	1	1	1	16383
0	≤ –V_{REF}	0	0	0	0	0	0	0

The LTC2460 (single-ended input) output code is a direct binary encoded result, see Table 1.

During the data output operation the $\overline{CS}$ input pin must be pulled low ($\overline{CS}$ = LOW). The data output process starts with the most significant bit of the result being present at the SDO output pin (SDO = D15) once $\overline{CS}$ goes low. A new data bit appears at the SDO output pin after each falling edge detected at the SCK input pin. The output data can be reliably latched on the rising edge of SCK.

Data Input Format

The data input word is 4 bits long and consists of two enable bits (EN1 and EN2) and two programming bits (SPD and SLP). EN1 is applied to the first rising edge of SCK after the conversion is complete. Programming is enabled by setting EN1 = 1 and EN2 = 0.

The speed bit (SPD) is only used by the LTC2460. In the default mode, SPD = 0, the output rate is 60Hz and continuous background offset calibration is not performed. By changing the SPD bit to 1, background offset calibration is performed and the output rate is reduced to 30Hz. Alternatively, SDI can be tied directly to ground (SPD = 0) or V_{CC} (SPD = 1), eliminating the need to program the device. The LTC2462 data output rate is always 60Hz and background offset calibration is performed (SPD = don't care).

The sleep bit (SLP) is used to power down the on chip reference. In the default mode, the reference remains powered up even when the ADC is powered down. If the SLP bit is set HIGH, the reference will power down after the next conversion is complete. It will remain powered down until $\overline{CS}$ is pulled low. The reference startup time is approximately 12ms. In order to ensure a stable reference for the following conversions, either the data input/output time should be delayed 12ms after $\overline{CS}$ goes low or the first conversion following a reference start up should be discarded. If SDI is tied HIGH (LTC2460 operating in 30Hz mode) the SLP mode is disabled.

Conversion Status Monitor

For certain applications, the user may wish to monitor the LTC2460/LTC2462 conversion status. This can be achieved by holding SCK HIGH during the conversion cycle. In this condition, whenever the $\overline{CS}$ input pin is pulled low ($\overline{CS}$ = LOW), the SDO output pin will provide an indication of the conversion status. SDO = HIGH is an indication of a conversion cycle in progress while SDO = LOW is an indication of a completed conversion cycle. An example of such a sequence is shown in Figure 5.

Conversion status monitoring, while possible, is not required for the LTC2460/LTC2462 as its conversion time is fixed and typically 16.6ms (23ms maximum). Therefore, external timing can be used to determine the completion of a conversion cycle.

SERIAL INTERFACE

The LTC2460/LTC2462 transmit the conversion result and receive the start of conversion command through a synchronous 2-, 3- or 4-wire interface. This interface can be

APPLICATIONS INFORMATION

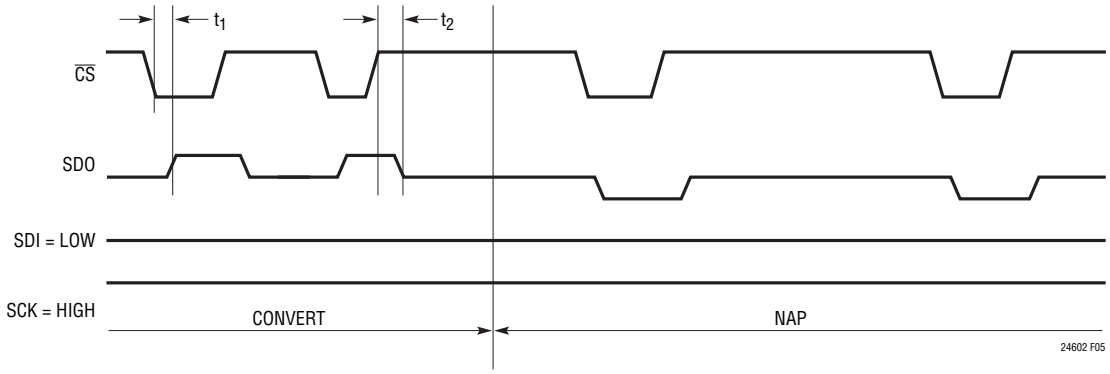


Figure 5. Conversion Status Monitoring Mode

used during the CONVERT and SLEEP states to assess the conversion status and during the DATA OUTPUT state to read the conversion result, and to trigger a new conversion.

Serial Interface Operation Modes

The modes of operation can be summarized as follows:

1) The LTC2460/LTC2462 function with SCK idle high (commonly known as CPOL = 1) or idle low (commonly known as CPOL = 0).

2) After the 16th bit is read, a new conversion is started if $\overline{CS}$ is pulled high or SCK is pulled low.

3) At any time during the Data Output state, pulling $\overline{CS}$ high causes the part to leave the I/O state, abort the output and begin a new conversion.

4) When SCK = HIGH, it is possible to monitor the conversion status by pulling $\overline{CS}$ low and watching for SDO to go low. This feature is available only in the idle-high (CPOL = 1) mode.

Serial Clock Idle-High (CPOL = 1) Examples

In Figure 6, following a conversion cycle the LTC2460/LTC2462 automatically enter the NAP mode with the ADC powered down. The ADC's reference will power down if the SLP bit was set high prior to the just completed conversion and $\overline{CS}$ is HIGH. Once $\overline{CS}$ goes low, the device powers up. The user can monitor the conversion status at convenient intervals using $\overline{CS}$ and SDO.

Pulling $\overline{CS}$ LOW while SCK is HIGH tests whether or not the chip is in the CONVERT state. While in the CONVERT state, SDO is HIGH while $\overline{CS}$ is LOW. Once the conversion is complete, SDO is LOW

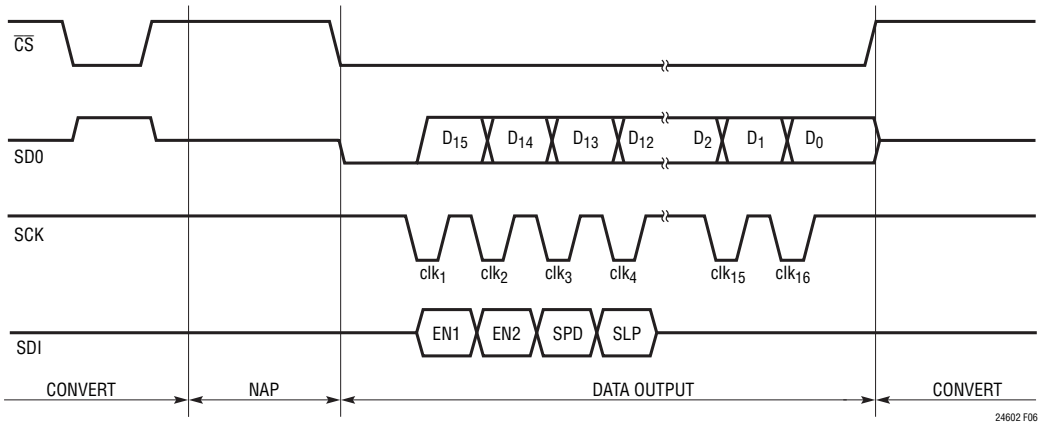


Figure 6. Idle-High (CPOL = 1) Serial Clock Operation Example. The Rising Edge of $\overline{CS}$ Starts a New Conversion

APPLICATIONS INFORMATION

while $\overline{CS}$ is LOW. These tests are not required operational steps but may be useful for some applications.

When the data is available, the user applies 16 clock cycles to transfer the result. The $\overline{CS}$ rising edge is then used to initiate a new conversion.

The operation example of Figure 7 is identical to that of Figure 6, except the new conversion cycle is triggered by the falling edge of the serial clock (SCK).

Serial Clock Idle-Low (CPOL = 0) Examples

In Figure 8, following a conversion cycle the LTC2460/LTC2462 automatically enters the NAP state. The device reference will power down if the SLP bit was set high prior to the just completed conversion and $\overline{CS}$ is HIGH. Once $\overline{CS}$ goes low, the reference powers up. The user determines data availability (and the end of conversion) based upon external timing. The user then pulls $\overline{CS}$ low ($\overline{CS}$ = ↓) and uses 16 clock cycles to transfer the result. Following the 16th rising edge of the clock, $\overline{CS}$ is pulled high ($\overline{CS}$ = ↑), which triggers a new conversion.

The timing diagram in Figure 9 is identical to that of Figure 8, except in this case a new conversion is triggered by SCK. The 16th SCK falling edge triggers a new conversion cycle and the $\overline{CS}$ signal is subsequently pulled high.

Examples of Aborting Cycle using $\overline{CS}$

For some applications, the user may wish to abort the I/O cycle and begin a new conversion. If the LTC2460/LTC2462 are in the data output state, a $\overline{CS}$ rising edge clears the remaining data bits from the output register, aborts the output cycle and triggers a new conversion. Figure 10 shows an example of aborting an I/O with idle-high (CPOL = 1) and Figure 11 shows an example of aborting an I/O with idle-low (CPOL = 0).

A new conversion cycle can be triggered using the $\overline{CS}$ signal without having to generate any serial clock pulses as shown in Figure 12. If SCK is maintained at a low logic level, after the end of a conversion cycle, a new conversion operation can be triggered by pulling $\overline{CS}$ low and then high. When $\overline{CS}$ is pulled low ($\overline{CS}$ = LOW), SDO will

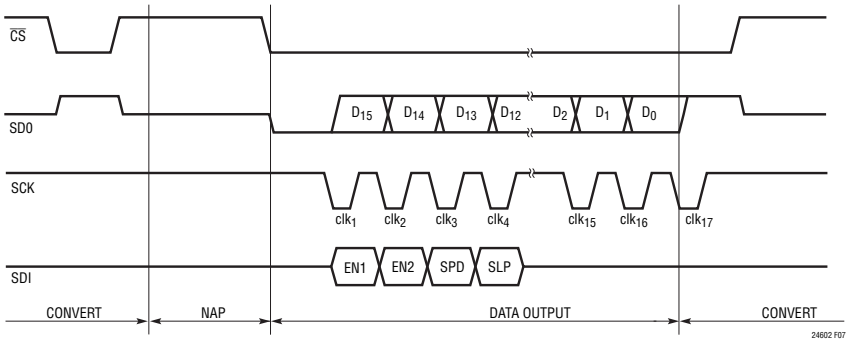


Figure 7. Idle-High (CPOL = 1) Clock Operation Example. A 17th Clock Pulse is Used to Trigger a New Conversion Cycle

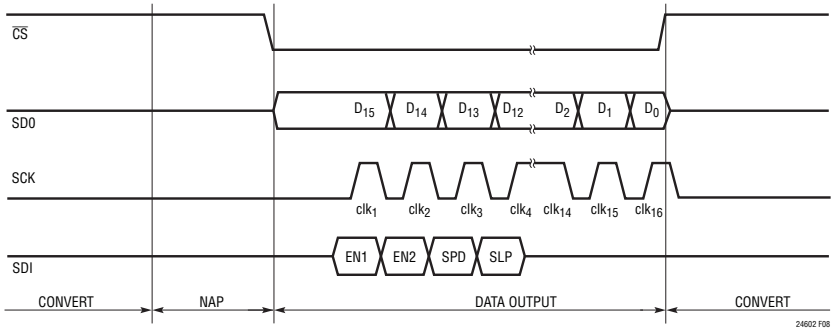


Figure 8. Idle-Low (CPOL = 0) Clock. $\overline{CS}$ Triggers a New Conversion

APPLICATIONS INFORMATION

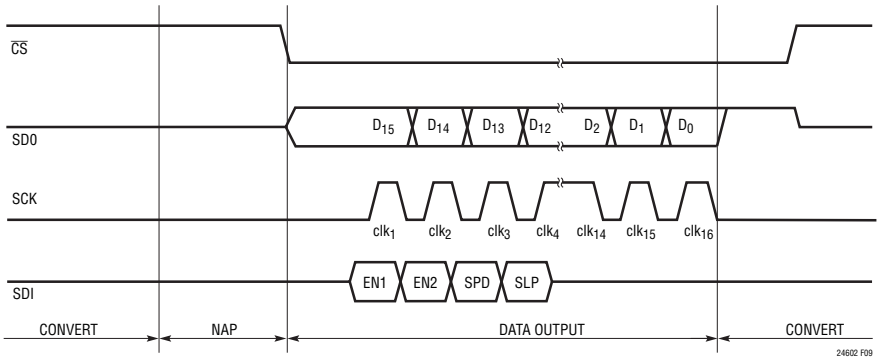


Figure 9. Idle-Low (CPOL = 0) Clock. The 16th SCK Falling Edge Triggers a New Conversion

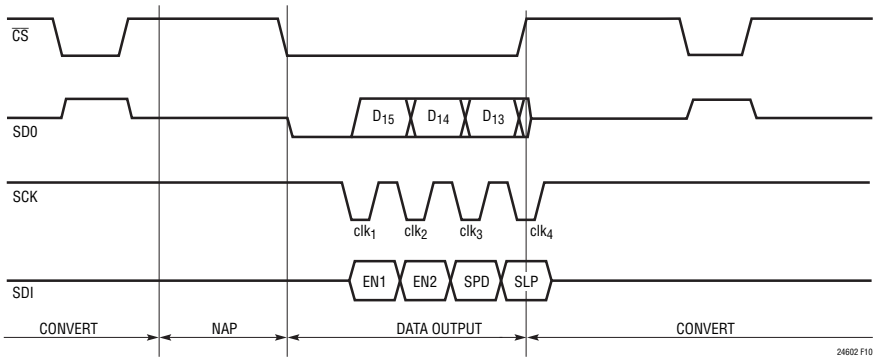


Figure 10. Idle-High (CPOL = 1) Clock and Aborted I/O Example

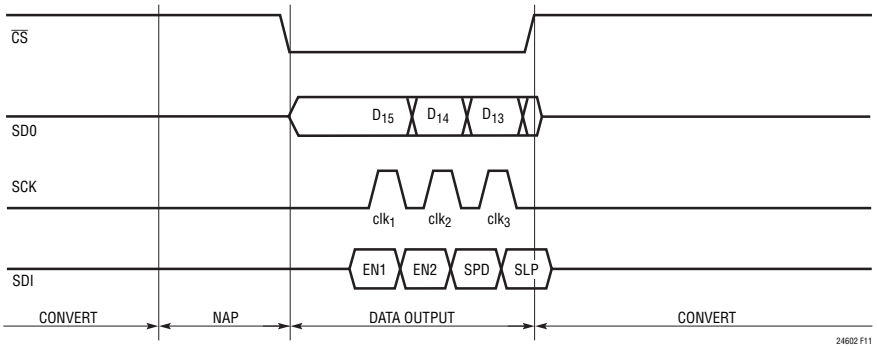


Figure 11. Idle-Low (CPOL = 0) Clock and Aborted I/O Example

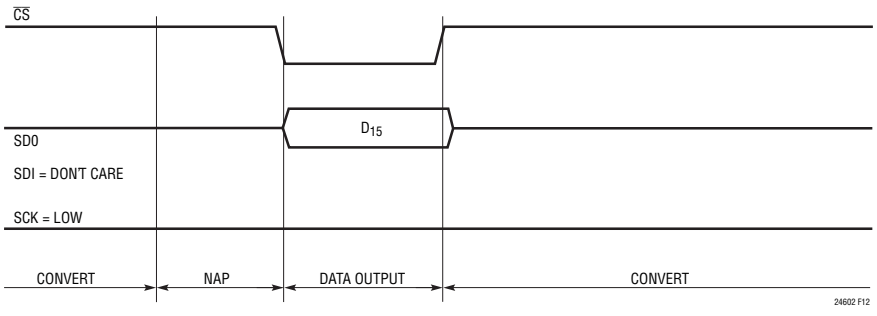


Figure 12. Idle-Low (CPOL = 0) Clock and Minimum Data Output Length Example

APPLICATIONS INFORMATION

output the sign (D15) of the result of the just completed conversion. While a low logic level is maintained at SCK pin and $\overline{CS}$ is subsequently pulled high ($\overline{CS}$ = HIGH) the remaining 15 bits of the result (D14:D0) are discarded and a new conversion cycle starts.

Following the aborted I/O, additional clock pulses in the CONVERT state are acceptable, but excessive signal transitions on SCK can potentially create noise on the ADC during the conversion, and thus may negatively influence the conversion accuracy.

2-Wire Operation

The 2-wire operation modes, while reducing the number of required control signals, should be used only if the LTC2460/LTC2462 low power sleep capability is not required. In addition the option to abort serial data transfers is no longer available. Hardwire $\overline{CS}$ to GND for 2-wire operation. For the LTC2460, tie SDI LOW for 60Hz output rate and HIGH for 30Hz output rate, for the LTC2462 tie SDI low.

Figure 13 shows a 2-wire operation sequence which uses an idle-high (CPOL = 1) serial clock signal. The conversion status can be monitored at the SDO output. Following a conversion cycle, the ADC enters the data output state and the SDO output transitions from HIGH to LOW. Subsequently 16 clock pulses are applied to the SCK input in order to serially shift the 16 bit result. Finally, the 17th clock pulse is applied to the SCK input in order to trigger a new conversion cycle.

Figure 14 shows a 2-wire operation sequence which uses an idle-low (CPOL = 0) serial clock signal. The conversion status cannot be monitored at the SDO output. Following a conversion cycle, the LTC2460/LTC2462 enters the DATA OUTPUT state. At this moment the SDO pin outputs the sign (D15) of the conversion result. The user must use external timing in order to determine the end of conversion and result availability. Subsequently 16 clock pulses are applied to SCK in order to serially shift the 16-bit result. The 16th clock falling edge triggers a new conversion cycle. For the LTC2460 tie SDI LOW for 60Hz output rate and HIGH for 30Hz output rate.

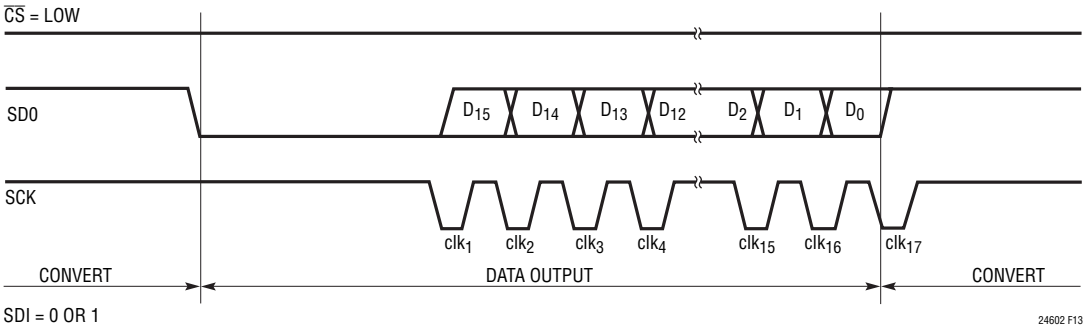


Figure 13. 2-Wire, Idle-High (CPOL = 1) Serial Clock, Operation Example

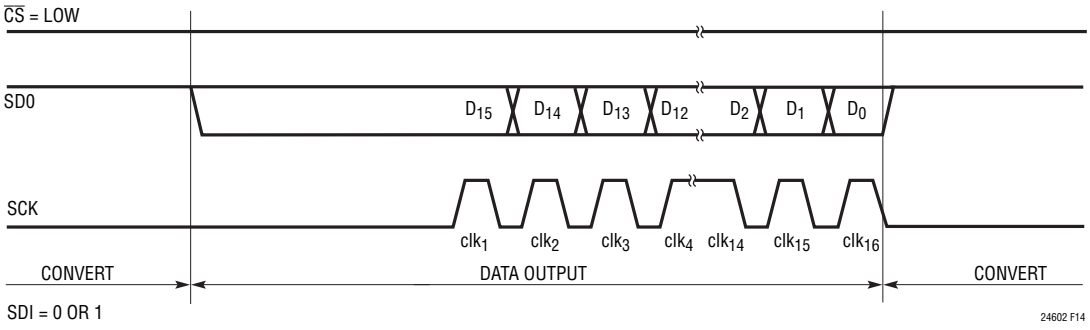


Figure 14. 2-Wire, Idle-Low (CPOL = 0) Serial Clock Operation Example

APPLICATIONS INFORMATION

PRESERVING THE CONVERTER ACCURACY

The LTC2460/LTC2462 are designed to minimize the conversion result's sensitivity to device decoupling, PCB layout, antialiasing circuits, line and frequency perturbations. Nevertheless, in order to preserve the high accuracy capability of this part, some simple precautions are desirable.

Digital Signal Levels

Due to the nature of CMOS logic, it is advisable to keep input digital signals near GND or V_{CC}. Voltages in the range of 0.5V to V_{CC} – 0.5V may result in additional current leakage from the part. Undershoot and overshoot should also be minimized, particularly while the chip is converting. It is thus beneficial to keep edge rates of about 10ns and limit overshoot and undershoot to less than 0.3V.

Noisy external circuitry can potentially impact the output under 2-wire operation. In particular, it is possible to get the LTC2460/LTC2462 into an unknown state if an SCK pulse is missed or noise triggers an extra SCK pulse. In this situation, it is impossible to distinguish SDO = 1 (indicating conversion in progress) from valid "1" data bits. As such, CPOL = 1 is recommended for the 2-wire mode. The user should look for SDO = 0 before reading data, and look for SDO = 1 after reading data. If SDO does not return a "0" within the maximum conversion time (or return a "1" after a full data read), generate 16 SCK pulses to force a new conversion.

Driving V_{CC} and GND

In relation to the V_{CC} and GND pins, the LTC2460/LTC2462 combines internal high frequency decoupling with damping elements, which reduce the ADC performance sensitivity to PCB layout and external components. Nevertheless, the very high accuracy of this converter is best preserved by careful low and high frequency power supply decoupling.

A 0.1µF, high quality, ceramic capacitor in parallel with a 10µF low ESR ceramic capacitor should be connected between the V_{CC} and GND pins, as close as possible to the package. The 0.1µF capacitor should be placed closest to the ADC package. It is also desirable to avoid any via in the circuit path, starting from the converter V_{CC} pin, passing through these two decoupling capacitors, and returning to the converter GND pin. The area encompassed by this circuit path, as well as the path length, should be minimized.

As shown in Figure 15, REF^- is used as the negative reference voltage input to the ADC. This pin can be tied directly to ground or kelvined to sensor ground. In the case where REF^- is used as a sense input, it should be bypassed to ground with a 0.1µF ceramic capacitor in parallel with a 10µF low ESR ceramic capacitor.

Very low impedance ground and power planes, and star connections at both V_{CC} and GND pins, are preferable. The V_{CC} pin should have two distinct connections: the first to the decoupling capacitors described above, and the second to the ground return for the power supply voltage source.

REFOUT and COMP

The on chip 1.25V reference is internally tied to the converter's reference input and is output to the REFOUT pin. A 0.1µF capacitor should be placed on the REFOUT pin. It is possible to reduce this capacitor, but the transition

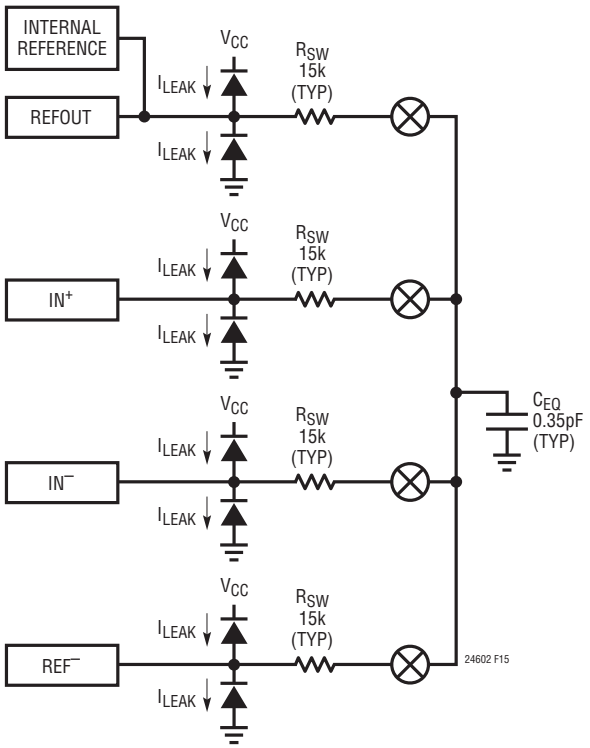


Figure 15. LTC2460/LTC2462 Analog Input/Reference Equivalent Circuit

APPLICATIONS INFORMATION

noise increases. A 0.1µF capacitor should also be placed on the COMP pin. This pin is tied to an internal point in the reference and is used for stability. In order for the reference to remain stable the capacitor placed on the COMP pin must be greater than or equal to the capacitor tied to the REFOUT pin. The REFOUT pin cannot be overridden by an external voltage. If a reference voltage greater than 1.25V is required, the LTC2450/LTC2452 should be used.

Depending on the size of the capacitors tied to the REFOUT and COMP pins, the internal reference has a corresponding start up time. This start up time is typically 12ms when 0.1µF capacitors are used. At initial power up, the first conversion result can be aborted or ignored. At the completion of this first conversion, the reference has settled and all subsequent conversions are valid.

If the reference is put to sleep (program SLP = 1 and $\overline{CS}$ = 1) the reference is powered down after the next conversion. This conversion result is valid. On $\overline{CS}$ falling edge, the reference is powered up. In order to ensure the reference output has settled before the next conversion, the power up time can be extended by delaying the data read 12ms after the falling edge of $\overline{CS}$. Once all 16 bits are read from the device or $\overline{CS}$ is brought HIGH, the next conversion automatically begins. In the default operation, the reference remains powered up at the conclusion of the conversion cycle.

Driving V_{IN}^+ and V_{IN}^-

The input drive requirements can best be analyzed using the equivalent circuit of Figure 16. The input signal V_{SIG} is connected to the ADC input pins (IN^+ and IN^-) through an equivalent source resistance R_S. This resistor includes both the actual generator source resistance and any additional optional resistors connected to the input pins. Optional input capacitors C_{IN} are also connected to the ADC input pins. This capacitor is placed in parallel with the ADC input parasitic capacitance C_{PAR}. Depending on the PCB layout, C_{PAR} has typical values between 2pF and 15pF. In addition, the equivalent circuit of Figure 16 includes the converter equivalent internal resistor R_{SW} and sampling capacitor C_{EQ}.

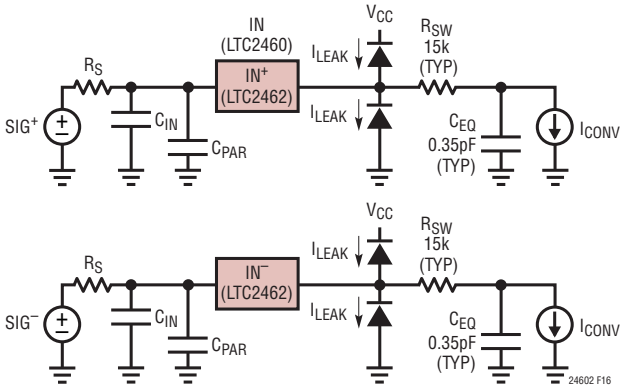


Figure 16. LTC2460/LTC2462 Input Drive Equivalent Circuit

There are some immediate trade-offs in R_S and C_{IN} without needing a full circuit analysis. Increasing R_S and C_{IN} can give the following benefits:

1) Due to the LTC2460/LTC2462's input sampling algorithm, the input current drawn by either V_{IN}^+ or V_{IN}^- over a conversion cycle is typically 50nA. A high $R_S \bullet C_{IN}$ attenuates the high frequency components of the input current, and R_S values up to 1k result in <1LSB error.
2) The bandwidth from V_{SIG} is reduced at the input pins (IN^+, IN^- or IN). This bandwidth reduction isolates the ADC from high frequency signals, and as such provides simple antialiasing and input noise reduction.
3) Switching transients generated by the ADC are attenuated before they go back to the signal source.
4) A large C_{IN} gives a better AC ground at the input pins, helping reduce reflections back to the signal source.
5) Increasing R_S protects the ADC by limiting the current during an outside-the-rails fault condition.

APPLICATIONS INFORMATION

There is a limit to how large $R_S \bullet C_{IN}$ should be for a given application. Increasing R_S beyond a given point increases the voltage drop across R_S due to the input current, to the point that significant measurement errors exist. Additionally, for some applications, increasing the $R_S \bullet C_{IN}$ product too much may unacceptably attenuate the signal at frequencies of interest.

For most applications, it is desirable to implement C_{IN} as a high-quality 0.1µF ceramic capacitor and $R_S \leq 1k$. This capacitor should be located as close as possible to the actual V_{IN} package pin. Furthermore, the area encompassed by this circuit path, as well as the path length, should be minimized.

In the case of a 2-wire sensor that is not remotely grounded, it is desirable to split R_S and place series resistors in the ADC input line as well as in the sensor ground return line, which should be tied to the ADC GND pin using a star connection topology.

Figure 17 shows the measured LTC2462 INL vs Input Voltage as a function of R_S value with an input capacitor $C_{IN} = 0.1\mu F$.

In some cases, R_S can be increased above these guidelines. The input current is zero when the ADC is either in sleep or I/O modes. Thus, if the time constant of the input RC circuit $\tau = R_S \bullet C_{IN}$, is of the same order of magnitude or longer than the time periods between actual conversions, then one can consider the input current to be reduced correspondingly.

These considerations need to be balanced out by the input signal bandwidth. The 3dB bandwidth $\approx 1/(2\pi R_S C_{IN})$.

Finally, if the recommended choice for C_{IN} is unacceptable for the user's specific application, an alternate strategy is to eliminate C_{IN} and minimize C_{PAR} and R_S. In practical terms, this configuration corresponds to a low impedance sensor directly connected to the ADC through minimum length traces. Actual applications include current measurements through low value sense resistors, temperature measurements, low impedance voltage source monitoring, and so on. The resultant INL vs V_{IN} is shown in Figure 18. The measurements of Figure 18 include a capacitor C_{PAR} corresponding to a minimum sized layout pad and a minimum width input trace of about 1 inch length.

Signal Bandwidth, Transition Noise and Noise Equivalent Input Bandwidth

The LTC2460/LTC2462 include a $sinc^1$ type digital filter with the first notch located at f_0 = 60Hz. As such, the 3dB input signal bandwidth is 26.54Hz. The calculated LTC2460/LTC2462 input signal attenuation vs frequency over a wide frequency range is shown in Figure 19. The calculated LTC2460/LTC2462 input signal attenuation vs frequency at low frequencies is shown in Figure 20. The converter noise level is about $2.2\mu V_{RMS}$ and can be modeled by a white noise source connected at the input of a noise-free converter.

On a related note, the LTC2462 uses two separate A/D converters to digitize the positive and negative inputs. Each of these A/D converters has $2.2\mu V_{RMS}$ transition noise. If one of the input voltages is within this small transition noise band, then the output will fluctuate one bit, regardless of the value of the other input voltage. If both of the input voltages are within their transition noise bands, the output can fluctuate 2 bits.

For a simple system noise analysis, the V_{IN} drive circuit can be modeled as a single-pole equivalent circuit characterized by a pole location f_i and a noise spectral density n_i. If the converter has an unlimited bandwidth, or at least a bandwidth substantially larger than f_i, then the total noise contribution of the external drive circuit would be:

$$V_n = n_i \sqrt{\pi / 2 \bullet f_i}$$

Then, the total system noise level can be estimated as the square root of the sum of (V_n^2) and the square of the LTC2460/LTC2462 noise floor (~$2.2\mu V^2$).

APPLICATIONS INFORMATION

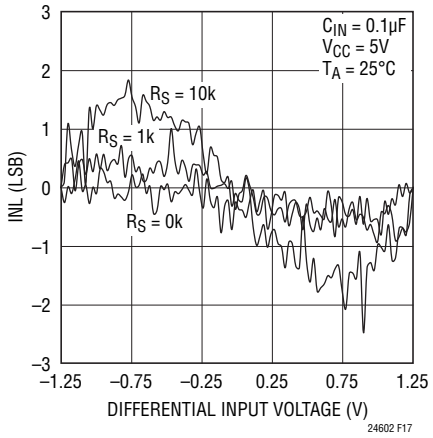


Figure 17. Measured INL vs Input Voltage

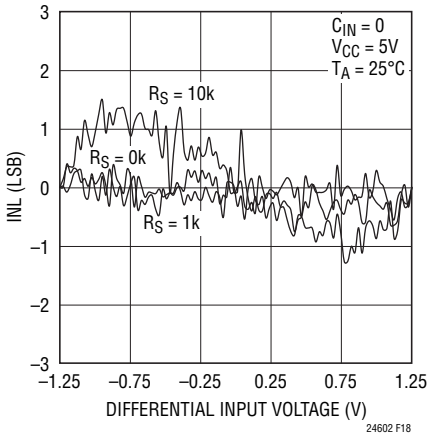


Figure 18. Measured INL vs Input Voltage

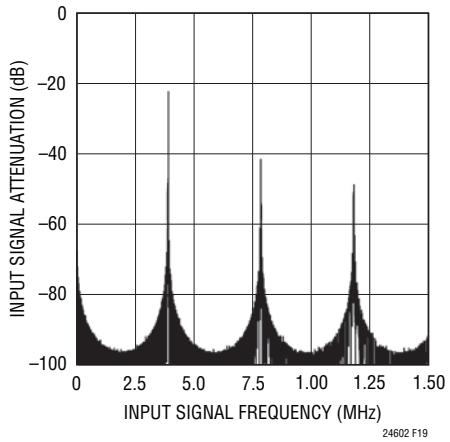


Figure 19. LTC2462 Input Signal Attentuation vs Frequency

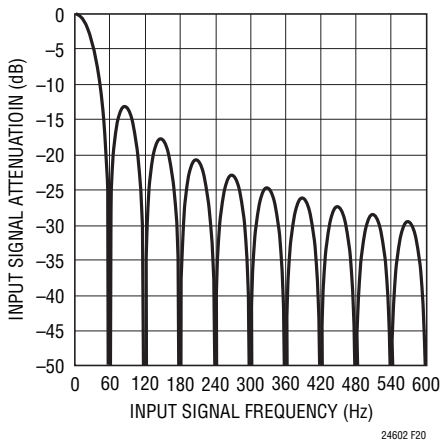
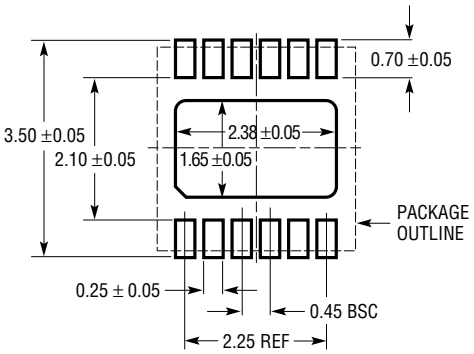


Figure 20. LTC2462 Input Signal Attenuation vs Frequency (Low Frequencies)

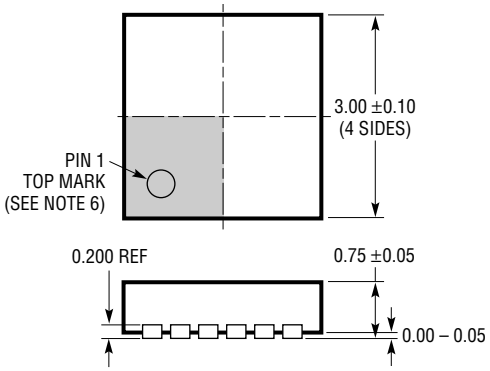
PACKAGE DESCRIPTION

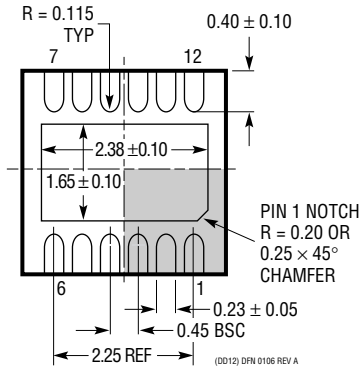
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
12-Lead Plastic DFN (3mm 3mm)
(Reference LTC DWG # 05-08-1725 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





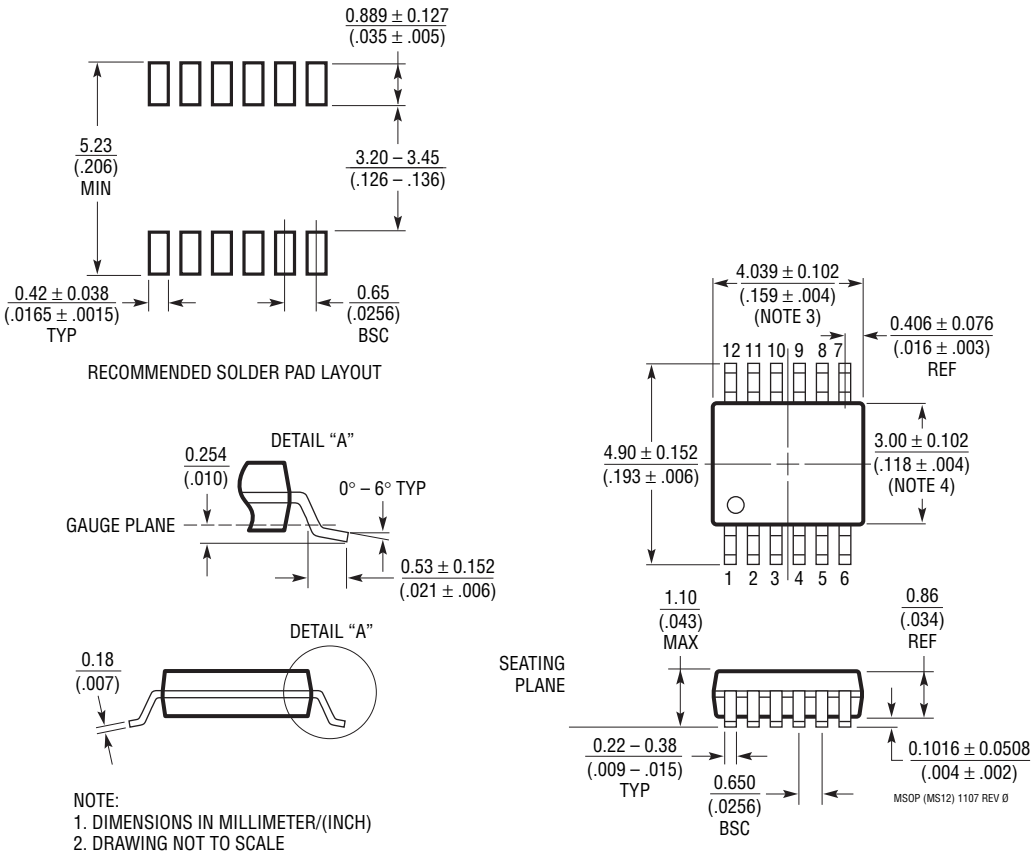
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD AND TIE BARS SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS Package
12-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1668 Rev Ø)

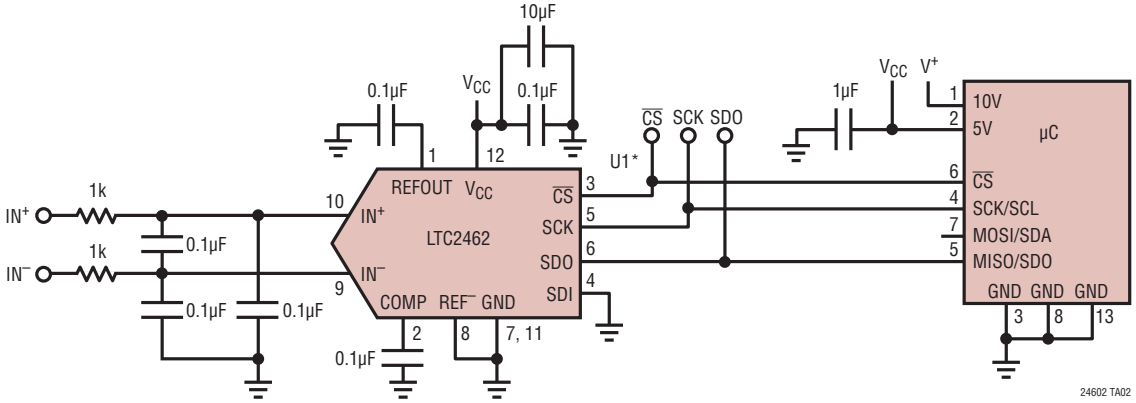


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/11	Updated Offset Error Maximum in the Electrical Characteristics table.	3

TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1860/LTC1861	12-Bit, 5V, 1-/2-Channel 250ksps SAR ADC in MSOP	850µA at 250ksps, 2µA at 1ksps, SO-8 and MSOP Packages
LTC1860L/LTC1861L	12-Bit, 3V, 1-/2-Channel 150ksps SAR ADC	450µA at 150ksps, 10µA at 1ksps, SO-8 and MSOP Packages
LTC1864/LTC1865	16-Bit, 5V, 1-/2-Channel 250ksps SAR ADC in MSOP	850µA at 250ksps, 2µA at 1ksps, SO-8 and MSOP Packages
LTC1864L/LTC1865L	16-bit, 3V, 1-/2-Channel 150ksps SAR ADC	450µA at 150ksps, 10µA at 1ksps, SO-8 and MSOP Packages
LTC2360	12-Bit, 100ksps SAR ADC	3V Supply, 1.5mW at 100ksps, TSOT 6-pin/8-pin Packages
LTC2440	24-Bit No Latency ΔΣ™ ADC	200nV$_{RMS}$ Noise, 4kHz Output Rate, 15ppm INL
LTC2480	16-Bit, Differential Input, No Latency ΔΣ ADC, with PGA, Temp. Sensor, SPI	Easy-Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2481	16-Bit, Differential Input, No Latency ΔΣ ADC, with PGA, Temp. Sensor, I^{2}C	Easy-Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2482	16-Bit, Differential Input, No Latency ΔΣ ADC, SPI	Easy-Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2483	16-Bit, Differential Input, No Latency ΔΣ ADC, I^{2}C	Easy-Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2484	24-Bit, Differential Input, No Latency ΔΣ ADC, SPI with Temp. Sensor	Easy-Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2485	24-Bit, Differential Input, No Latency ΔΣ ADC, I^{2}C with Temp. Sensor	Easy-Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC6241	Dual, 18MHz, Low Noise, Rail-to-Rail Op Amp	550nV$_{P-P}$ Noise, 125µV Offset Max
LTC2450	Easy-to-Use, Ultra-Tiny 16-Bit ADC, SPI, 0V to 5.5V Input Range	2 LSB INL, 50nA Sleep current, Tiny 2mm × 2mm DFN-6 Package, 30Hz Output Rate
LTC2450-1	Easy-to-Use, Ultra-Tiny 16-Bit ADC, SPI, 0V to 5.5V Input Range	2 LSB INL, 50nA Sleep Current, Tiny 2mm × 2mm DFN-6 Package, 60Hz Output Rate
LTC2451	Easy-to-Use, Ultra-Tiny 16-Bit ADC, I^{2}C, 0V to 5.5V Input Range	2 LSB INL, 50nA Sleep Current, Tiny 3mm × 2mm DFN-8 or TSOT Package, Programmable 30Hz/60Hz Output Rates
LTC2452	Easy-to-Use, Ultra-Tiny 16-Bit Differential ADC, SPI, ±5.5V Input Range	2 LSB INL, 50nA Sleep Current, Tiny 3mm × 2mm DFN-8 or TSOT Package
LTC2453	Easy-to-Use, Ultra-Tiny 16-Bit Differential ADC, I^{2}C, ±5.5V Input Range	2 LSB INL, 50nA Sleep Current, Tiny 3mm × 2mm DFN-8 or TSOT Package

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0911 REV A • PRINTED IN USA