LTC2162

16-Bit, 65Msps Low Power ADCs

FEATURES

- 77dB SNR
- 90dB SFDR
- Low Power: 87mW/63mW/45mW
- Single 1.8V Supply
- CMOS, DDR CMOS, or DDR LVDS Outputs
- Selectable Input Ranges: $1V_{P-P}$ to $2V_{P-P}$
- 550MHz Full Power Bandwidth S/H
- Optional Data Output Randomizer
- Optional Clock Duty Cycle Stabilizer
- Shutdown and Nap Modes
- Serial SPI Port for Configuration
- 48-Pin (7mm × 7mm) QFN Package

APPLICATIONS

- Communications
- Cellular Base Stations
- Software Defined Radios
- Portable Medical Imaging
- Multichannel Data Acquisition
- Nondestructive Testing

DESCRIPTION

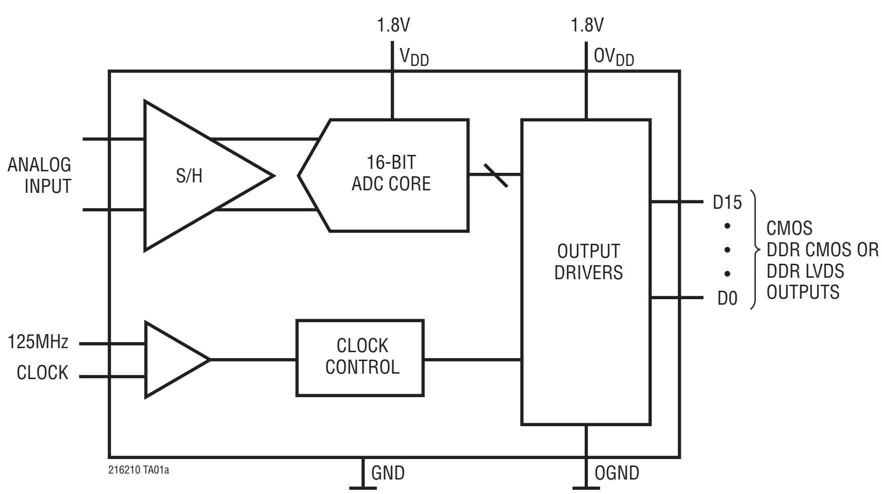
The LTC®2162/LTC2161/LTC2160 are sampling 16-bit A/D converters designed for digitizing high frequency, wide dynamic range signals. They are perfect for demanding communications applications with AC performance that includes 77dB SNR and 90dB spurious free dynamic range (SFDR). Ultralow jitter of $0.07ps_{RMS}$ allows undersampling of IF frequencies with excellent noise performance.

DC specs include ±2LSB INL (typ), ±0.5LSB DNL (typ) and no missing codes over temperature. The transition noise is $3.3LSB_{RMS}$.

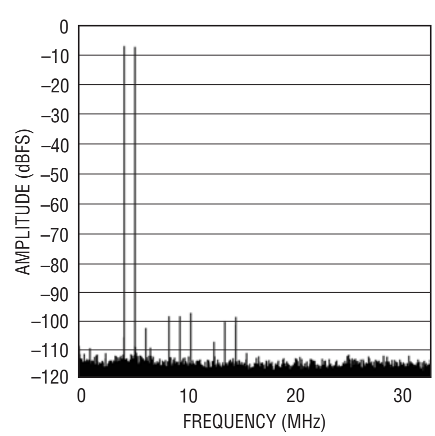
The digital outputs can be either full rate CMOS, double data rate CMOS, or double data rate LVDS. A separate output power supply allows the CMOS output swing to range from 1.2V to 1.8V.

The ENC^+ and $ENC^–$ inputs may be driven differentially or single-ended with a sine wave, PECL, LVDS, TTL, or CMOS inputs. An optional clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.

TYPICAL APPLICATION



2-Tone FFT, f_{IN} = 70MHz and 69MHz



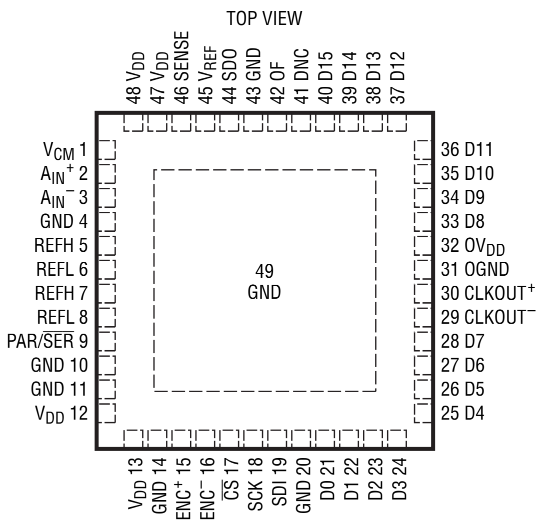
ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltages (V_{DD}, O_{VDD}) .... –0.3V to 2V
Analog Input Voltage (A_{IN}^+, A_{IN}^-, PAR/$\overline{SER}$, SENSE)
(Note 3) .... –0.3V to (V_{DD} + 0.2V)
Digital Input Voltage (ENC^+, ENC^-, $\overline{CS}$, SDI, SCK)
(Note 4) .... –0.3V to 3.9V
SDO (Note 4).. –0.3V to 3.9V

Digital Output Voltage .... –0.3V to (OV_{DD} + 0.3V)
Operating Temperature Range
LTC2162C, LTC2161C, LTC2160C............. 0°C to 70°C
LTC2162I, LTC2161I, LTC2160I .... –40°C to 85°C
Storage Temperature Range .... –65°C to 150°C

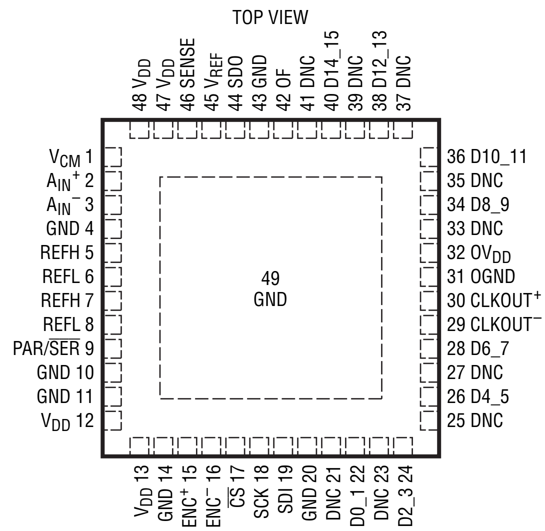
PIN CONFIGURATION

FULL RATE CMOS OUTPUT MODE



UK PACKAGE
48-LEAD (7mm × 7mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 29°C/W
EXPOSED PAD (PIN 49) IS GND, MUST BE SOLDERED TO PCB

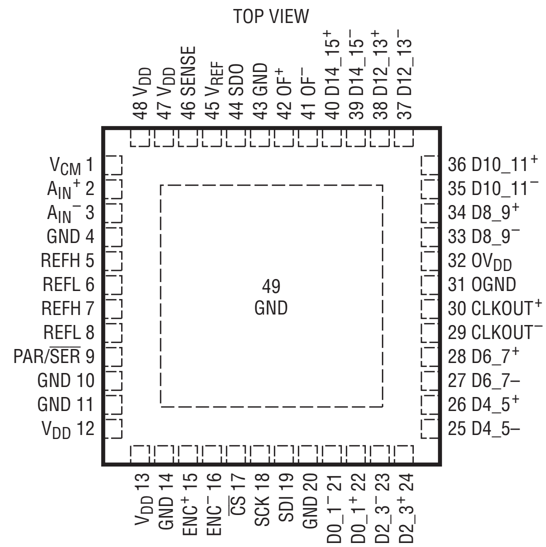
DOUBLE DATA RATE CMOS OUTPUT MODE



UK PACKAGE
48-LEAD (7mm × 7mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 29°C/W
EXPOSED PAD (PIN 49) IS GND, MUST BE SOLDERED TO PCB

PIN CONFIGURATION

DOUBLE DATA RATE LVDS OUTPUT MODE



UK PACKAGE
48-LEAD (7mm × 7mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 29°C/W
EXPOSED PAD (PIN 49) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2162CUK#PBF	LTC2162CUK#TRPBF	LTC2162UK	48-Lead (7mm × 7mm) Plastic QFN	0°C to 70°C
LTC2162IUK#PBF	LTC2162IUK#TRPBF	LTC2162UK	48-Lead (7mm × 7mm) Plastic QFN	–40°C to 85°C
LTC2161CUK#PBF	LTC2161CUK#TRPBF	LTC2161UK	48-Lead (7mm × 7mm) Plastic QFN	0°C to 70°C
LTC2161IUK#PBF	LTC2161IUK#TRPBF	LTC2161UK	48-Lead (7mm × 7mm) Plastic QFN	–40°C to 85°C
LTC2160CUK#PBF	LTC2160CUK#TRPBF	LTC2160UK	48-Lead (7mm × 7mm) Plastic QFN	0°C to 70°C
LTC2160IUK#PBF	LTC2160IUK#TRPBF	LTC2160UK	48-Lead (7mm × 7mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		LTC2162 MIN	LTC2162 TYP	LTC2162 MAX	LTC2161 MIN	LTC2161 TYP	LTC2161 MAX	LTC2160 MIN	LTC2160 TYP	LTC2160 MAX	UNITS
Resolution (No Missing Codes)		●	16			16			16			Bits
Integral Linearity Error	Differential Analog Input (Note 6)	●	–6	±2	6	–6	±2	6	–6	±2	6	LSB
Differential Linearity Error	Differential Analog Input	●	–0.9	±0.5	0.9	–0.9	±0.5	0.9	–0.9	±0.5	0.9	LSB
Offset Error	(Note 7)	●	–7	±1.5	7	–7	±1.5	7	–7	±1.5	7	mV
Gain Error	Internal Reference External Reference	 ●	 –1.8	±1.5 –0.5	 0.8	 –1.8	±1.5 –0.5	 0.8	 –1.8	±1.5 –0.5	 0.8	%FS %FS
Offset Drift				±10			±10			±10		µV/°C
Full-Scale Drift	Internal Reference External Reference			±30 ±10			±30 ±10			±30 ±10		ppm/°C ppm/°C
Transition Noise	External Reference			3.3			3.3			3.2		LSB_{RMS}

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range ($A_{IN}^+ – A_{IN}^–$)	1.7V < V_{DD} < 1.9V	●		1 to 2		V_{P-P}
$V_{IN(CM)}$	Analog Input Common Mode ($A_{IN}^+ + A_{IN}^–$)/2	Differential Analog Input (Note 8)	●	0.7	V_{CM}	1.25	V
V_{SENSE}	External Voltage Reference Applied to SENSE	External Reference Mode	●	0.625	1.250	1.300	V
I_{INCM}	Analog Input Common Mode Current	Per Pin, 65Msps Per Pin, 40Msps Per Pin, 25Msps			104 64 40		µA µA µA
I_{IN1}	Analog Input Leakage Current (No Encode)	0 < A_{IN}^+, $A_{IN}^–$ < V_{DD}	●	–1		1	µA
I_{IN2}	PAR/$\overline{SER}$ Input Leakage Current	0 < PAR/$\overline{SER}$ < V_{DD}	●	–3		3	µA
I_{IN3}	SENSE Input Leakage Current	0.625 < SENSE < 1.3V	●	–3		3	µA
t_{AP}	Sample-and-Hold Acquisition Delay Time				0		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Jitter	Single-Ended Encode Differential Encode			0.07 0.09		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio				80		dB
BW-3B	Full Power Bandwidth	Figure 6 Test Circuit			550		MHz

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC2162 MIN	LTC2162 TYP	LTC2162 MAX	LTC2161 MIN	LTC2161 TYP	LTC2161 MAX	LTC2160 MIN	LTC2160 TYP	LTC2160 MAX	UNITS
SNR	Signal-to-Noise Ratio	5MHz Input 30MHz Input 70MHz Input 140MHz Input	 ● 	 75.4 	77.0 76.9 76.8 76.3		 75.3 	76.9 76.8 76.7 76.2		 75.5 	77.1 77.0 76.9 76.4		dBFS dBFS dBFS dBFS
SFDR	Spurious Free Dynamic Range 2nd Harmonic	5MHz Input 30MHz Input 70MHz Input 140MHz Input	 ● 	 82 	90 90 89 84		 83 	90 90 89 84		 83 	90 90 89 84		dBFS dBFS dBFS dBFS

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 5)

				LTC2162			LTC2161			LTC2160			
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
SFDR	Spurious Free Dynamic Range 3rd Harmonic	5MHz Input 30MHz Input 70MHz Input 140MHz Input	●	 83	90 90 89 84		 84	90 90 89 84		 84	90 90 89 84		dBFS dBFS dBFS dBFS
SFDR	Spurious Free Dynamic Range 4th Harmonic or Higher	5MHz Input 30MHz Input 70MHz Input 140MHz Input	●	 88	95 95 95 95		 89	95 95 95 95		 89	95 95 95 95		dBFS dBFS dBFS dBFS
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	5MHz Input 30MHz Input 70MHz Input 140MHz Input	●	 75	76.8 76.7 76.4 76.3		 75	76.7 76.6 76.3 75.2		 74.9	76.9 76.8 76.5 76.4		dBFS dBFS dBFS dBFS

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	I_{OUT} = 0	0.5•V_{DD} – 25mV	0.5•V_{DD}	0.5•V_{DD} + 25mV	V
V_{CM} Output Temperature Drift			±25		ppm/°C
V_{CM} Output Resistance	–600µA < I_{OUT} < 1mA		4		Ω
V_{REF} Output Voltage	I_{OUT} = 0	1.225	1.250	1.275	V
V_{REF} Output Temperature Drift			±25		ppm/°C
V_{REF} Output Resistance	–400µA < I_{OUT} < 1mA		7		Ω
V_{REF} Line Regulation	1.7V < V_{DD} < 1.9V		0.6		mV/V

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ENCODE INPUTS (ENC^+, $ENC^–$)							
DIFFERENTIAL ENCODE MODE ($ENC^–$ NOT TIED TO GND)							
V_{ID}	Differential Input Voltage	(Note 8)	●	0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set Externally Set (Note 8)	 ●	 1.1	1.2	 1.6	V V
V_{IN}	Input Voltage Range	ENC^+, $ENC^–$ to GND	●	0.2		3.6	V
R_{IN}	Input Resistance	(See Figure 10)			10		kΩ
C_{IN}	Input Capacitance	(Note 8)			3.5		pF
SINGLE-ENDED ENCODE MODE ($ENC^–$ TIED TO GND)							
V_{IH}	High Level Input Voltage	V_{DD} = 1.8V	●	1.2			V
V_{IL}	Low Level Input Voltage	V_{DD} = 1.8V	●			0.6	V
V_{IN}	Input Voltage Range	ENC^+ to GND	●	0		3.6	V
R_{IN}	Input Resistance	(See Figure 11)			30		kΩ
C_{IN}	Input Capacitance	(Note 8)			3.5		pF

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS (CS, SDI, SCK in Serial or Parallel Programming Mode. SDO in Parallel Programming Mode)							
V_{IH}	High Level Input Voltage	V_{DD} = 1.8V	●	1.3			V
V_{IL}	Low Level Input Voltage	V_{DD} = 1.8V	●			0.6	V
I_{IN}	Input Current	V_{IN} = 0V to 3.6V	●	–10		10	µA
C_{IN}	Input Capacitance	(Note 8)			3		pF
SDO OUTPUT (Serial Programming Mode. Open Drain Output. Requires 2kΩ Pull-Up Resistor if SDO is Used)							
R_{OL}	Logic Low Output Resistance to GND	V_{DD} = 1.8V, SDO = 0V			200		Ω
I_{OH}	Logic High Output Leakage Current	SDO = 0V to 3.6V	●	–10		10	µA
C_{OUT}	Output Capacitance	(Note 8)			3		pF
DIGITAL DATA OUTPUTS (CMOS MODES: FULL DATA RATE AND DOUBLE DATA RATE)							
OV_{DD} = 1.8V							
V_{OH}	High Level Output Voltage	I_O = –500µA	●	1.750	1.790		V
V_{OL}	Low Level Output Voltage	I_O = 500µA	●		0.010	0.050	V
OV_{DD} = 1.5V							
V_{OH}	High Level Output Voltage	I_O = –500µA			1.488		V
V_{OL}	Low Level Output Voltage	I_O = 500µA			0.010		V
OV_{DD} = 1.2V							
V_{OH}	High Level Output Voltage	I_O = –500µA			1.185		V
V_{OL}	Low Level Output Voltage	I_O = 500µA			0.010		V
DIGITAL DATA OUTPUTS (LVDS MODE)							
V_{OD}	Differential Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	●	247	350 175	454	mV mV
V_{OS}	Common Mode Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	●	1.125	1.250 1.250	1.375	V V
R_{TERM}	On-Chip Termination Resistance	Termination Enabled, OV_{DD} = 1.8V			100		Ω

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		LTC2162			LTC2161			LTC2160			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
CMOS Output Modes: Full Data Rate and Double Data Rate													
V_{DD}	Analog Supply Voltage	(Note 10)	●	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
OV_{DD}	Output Supply Voltage	(Note 10)	●	1.1	1.8	1.9	1.1	1.8	1.9	1.1	1.8	1.9	V
I_{VDD}	Analog Supply Current	DC Input Sine Wave Input	●		48.3 49.6	54		35.2 35.8	39		25.0 25.4	28.5	mA mA
I_{OVDD}	Digital Supply Current	Sine Wave Input, OV_{DD} =1.2V			2.6			1.6			1.0		mA
P_{DISS}	Power Dissipation	DC Input Sine Wave Input, OV_{DD} =1.2V	●		87 92	97.5		63 66	70.5		45 47	51.5	mW mW
LVDS Output Mode													
V_{DD}	Analog Supply Voltage	(Note 10)	●	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
OV_{DD}	Output Supply Voltage	(Note 10)	●	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9)

				LTC2162			LTC2161			LTC2160			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
I_{VDD}	Analog Supply Current	Sine Wave Input 1.75mA Mode 3.5mA Mode	 ●		50.3 51.1	 57		37.3 38.2	 42		26.8 27.7	 31	mA mA
I_{OVDD}	Digital Supply Current (OV_{DD} = 1.8V)	Sine Wave Input 1.75mA Mode 3.5mA Mode	 ●		21.5 41.2	 46		21.4 41.1	 46		21.1 40.9	 46	mA mA
P_{DISS}	Power Dissipation	Sine Wave Input, 1.75mA Mode Sine Wave Input, 3.5mA Mode	 ●		129 166	 186		106 143	 159		86 123	 139	mW mW
All Output Modes													
P_{SLEEP}	Sleep Mode Power				1			1			1		mW
P_{NAP}	Nap Mode Power				10			10			10		mW
$P_{DIFFCLK}$	Power Increase with Differential Encode Mode Enabled (No Increase for Nap or Sleep Modes)				20			20			20		mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

				LTC2162			LTC2161			LTC2160			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
f_S	Sampling Frequency	(Note 10)	●	1		65	1		40	1		25	MHz
t_L	ENC Low Time (Note 8)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	7.3 2	7.69 7.69	500 500	11.88 2	12.5 12.5	500 500	19 2	20 20	500 500	ns ns
t_H	ENC High Time (Note 8)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	7.3 2	7.69 7.69	500 500	11.88 2	12.5 12.5	500 500	19 2	20 20	500 500	ns ns
t_{AP}	Sample-and-Hold Acquisition Delay Time				0			0			0		ns

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL DATA OUTPUTS (CMOS MODES: FULL DATA RATE AND DOUBLE DATA RATE)							
t_D	ENC to Data Delay	C_L = 5pF (Note 8)	●	1.1	1.7	3.1	ns
t_C	ENC to CLKOUT Delay	C_L = 5pF (Note 8)	●	1	1.4	2.6	ns
t_{SKEW}	DATA to CLKOUT Skew	$t_D - t_C$ (Note 8)	●	0	0.3	0.6	ns
	Pipeline Latency	Full Data Rate Mode Double Data Rate Mode			6 6.5		Cycles Cycles
DIGITAL DATA OUTPUTS (LVDS MODE)							
t_D	ENC to Data Delay	C_L = 5pF (Note 8)	●	1.1	1.8	3.2	ns
t_C	ENC to CLKOUT Delay	C_L = 5pF (Note 8)	●	1	1.5	2.7	ns
t_{SKEW}	DATA to CLKOUT Skew	$t_D - t_C$ (Note 8)	●	0	0.3	0.6	ns
	Pipeline Latency				6.5		Cycles
SPI PORT TIMING (Note 8)							
t_{SCK}	SCK Period	Write Mode Readback Mode, C_{SDO} = 20pF, R_{PULLUP} = 2k	● ●	40 250			ns ns
t_S	$\overline{CS}$ to SCK Setup Time		●	5			ns
t_H	SCK to $\overline{CS}$ Setup Time		●	5			ns
t_{DS}	SDI Setup Time		●	5			ns
t_{DH}	SDI Hold Time		●	5			ns
t_{DO}	SCK Falling to SDO Valid	Readback Mode, C_{SDO} = 20pF, R_{PULLUP} = 2k	●			125	ns

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND with GND and OGND shorted (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below GND they will be clamped by internal diodes. When these pin voltages are taken above V_{DD} they will not be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND without latchup.

Note 5: V_{DD} = OV_{DD} = 1.8V, f_{SAMPLE} = 65MHz (LTC2162), 40MHz (LTC2161), or 25MHz (LTC2160), LVDS outputs, differential ENC^+/ENC^- = $2V_{P-P}$ sine wave, input range = $2V_{P-P}$ with differential drive, unless otherwise noted.

Note 6: Integral nonlinearity is defined as the deviation of a code from a best fit straight line to the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Offset error is the offset voltage measured from –0.5 LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111 in 2's complement output mode.

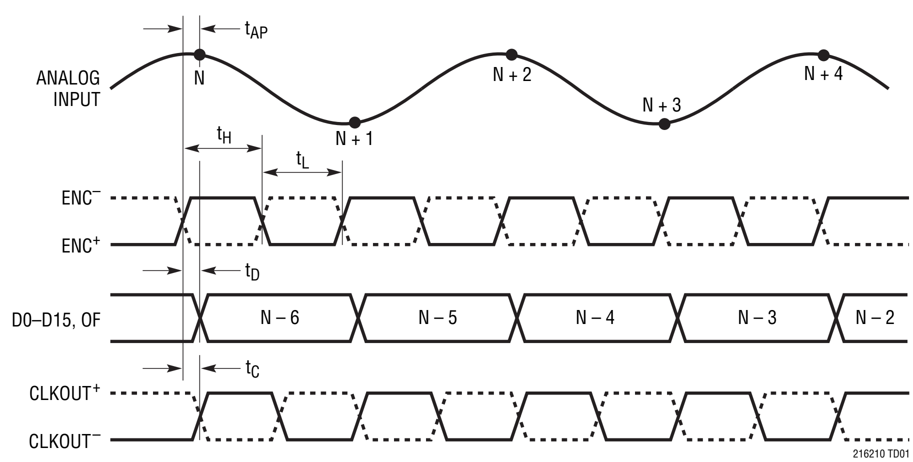
Note 8: Guaranteed by design, not subject to test.

Note 9: V_{DD} = 1.8V, f_{SAMPLE} = 65MHz (LTC2162), 40MHz (LTC2161), or 25MHz (LTC2160), CMOS outputs, ENC^+ = single-ended 1.8V square wave, ENC^- = 0V, input range = $2V_{P-P}$ with differential drive, 5pF load on each digital output unless otherwise noted.

Note 10: Recommended operating conditions.

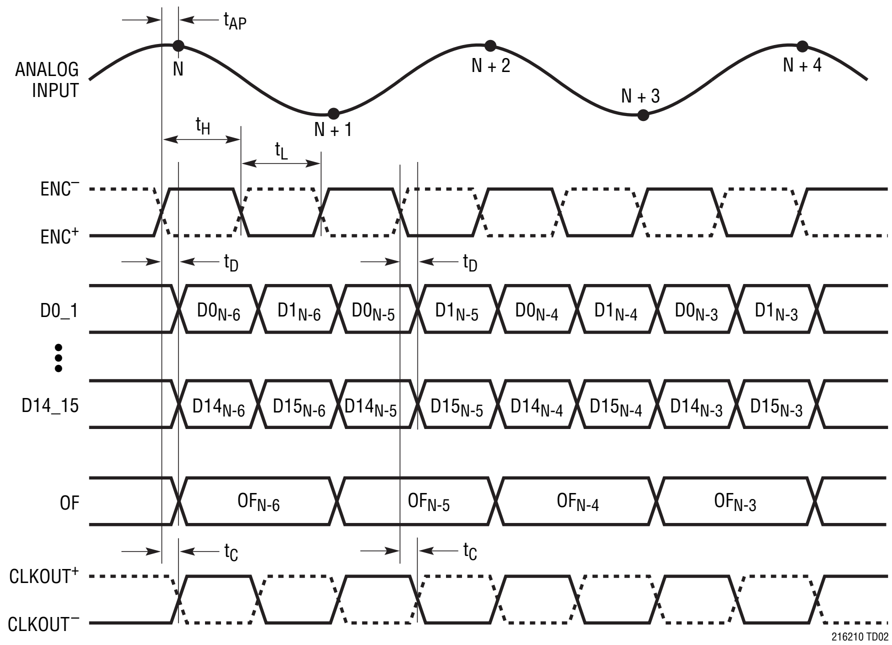
TIMING DIAGRAMS

Full-Rate CMOS Output Mode Timing
All Outputs are Single-Ended and Have CMOS Levels

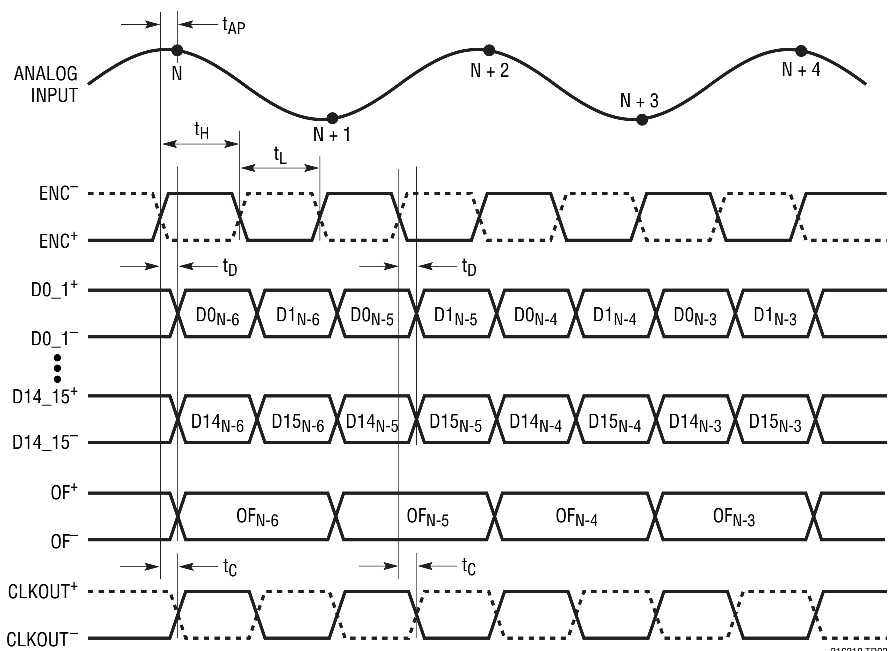


TIMING DIAGRAMS

Double Data Rate CMOS Output Mode Timing
All Outputs are Single-Ended and Have CMOS Levels

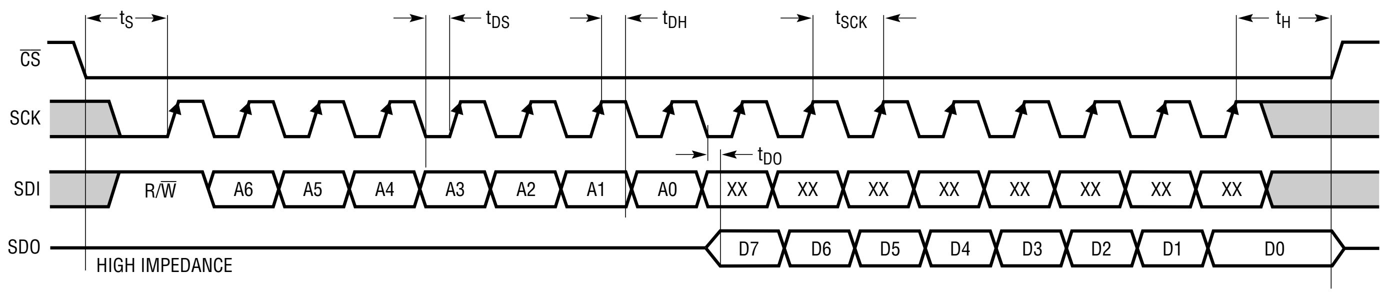


Double Data Rate LVDS Output Mode Timing
All Outputs are Differential and Have LVDS Levels

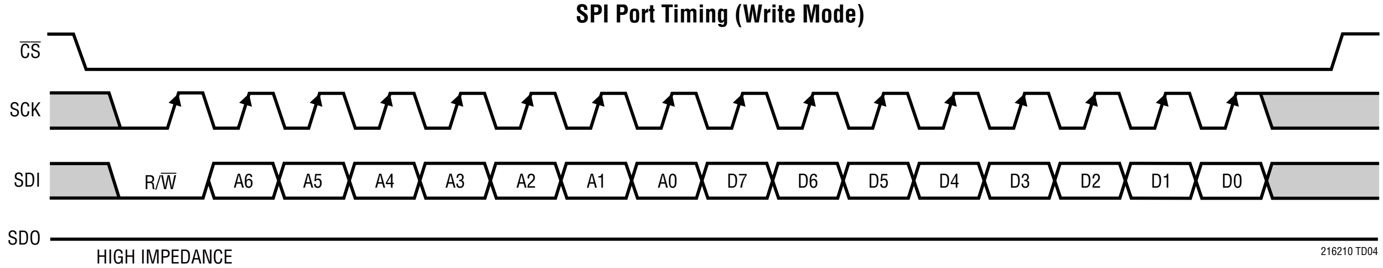


TIMING DIAGRAMS

SPI Port Timing (Readback Mode)



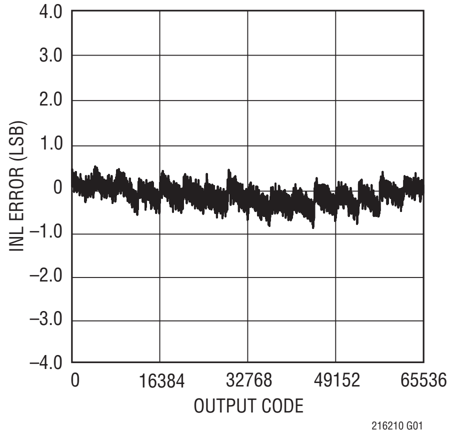
SPI Port Timing (Write Mode)



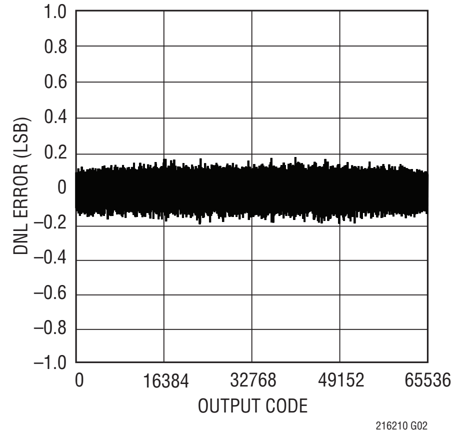
216210f

TYPICAL PERFORMANCE CHARACTERISTICS

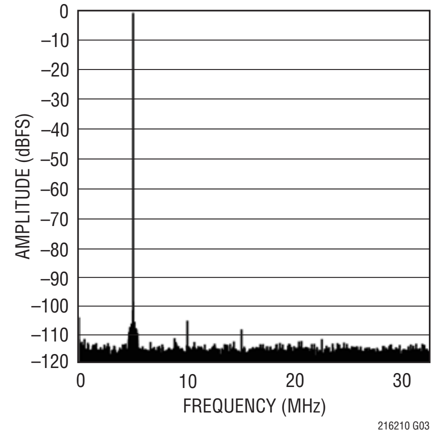
LTC2162: Integral Non-Linearity (INL)



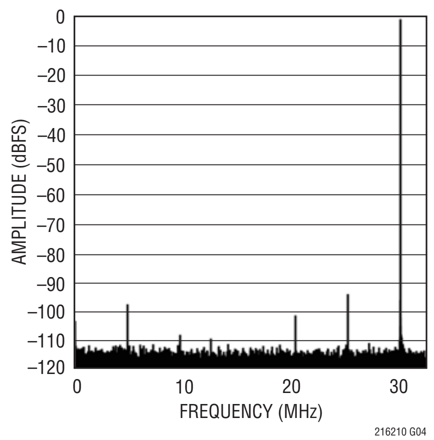
LTC2162: Differential Non-Linearity (DNL)



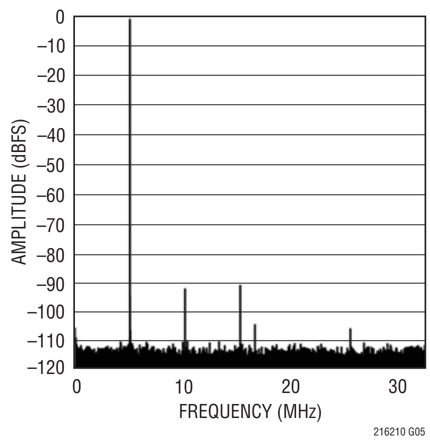
LTC2162: 64k Point FFT, f_{IN} = 5MHz –1dBFS, 65Msps



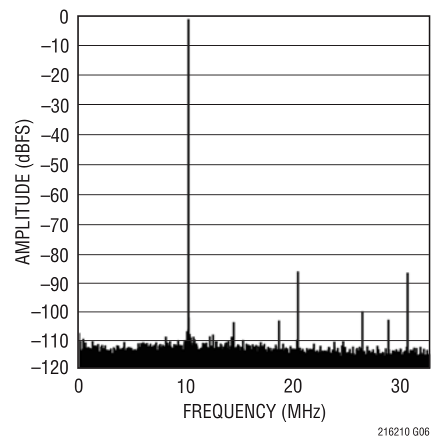
LTC2162: 64k Point FFT, f_{IN} = 30MHz, –1dBFS, 65Msps



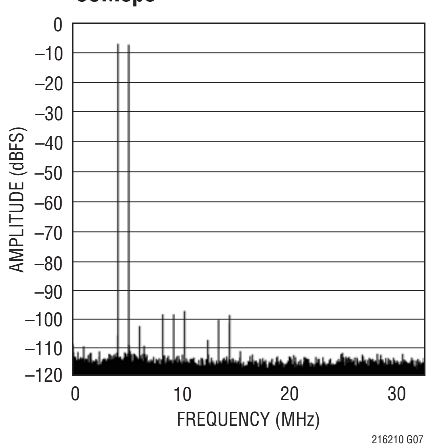
LTC2162: 64k Point FFT, f_{IN} = 70MHz, –1dBFS, 65Msps



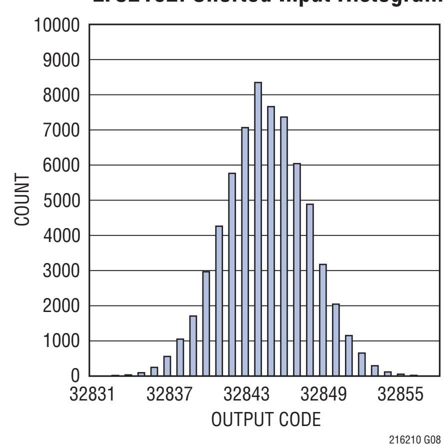
LTC2162: 64k Point FFT, f_{IN} = 140MHz, –1dBFS, 65Msps



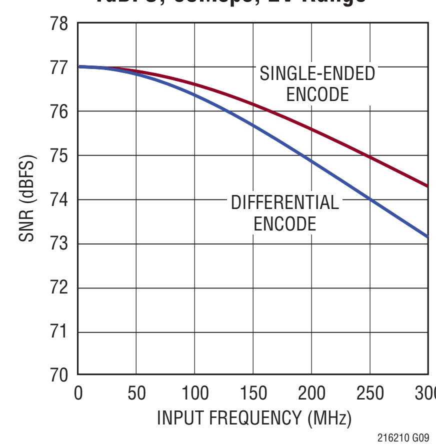
LTC2162: 64k Point 2-Tone FFT, f_{IN} = 69MHz, 70MHz, –7dBFS, 65Msps



LTC2162: Shorted Input Histogram

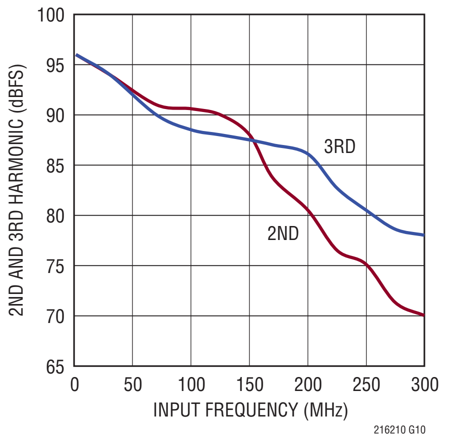


LTC2162: SNR vs Input Frequency, –1dBFS, 65Msps, 2V Range

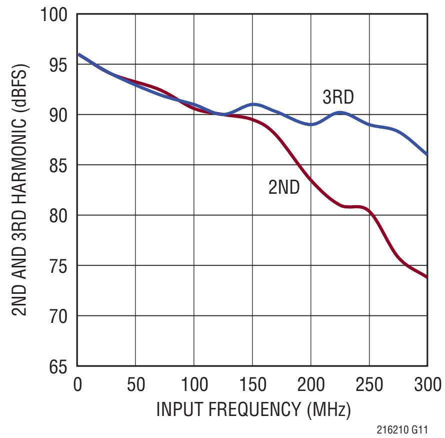


TYPICAL PERFORMANCE CHARACTERISTICS

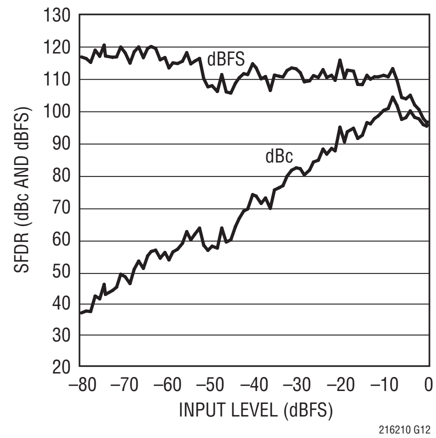
LTC2162: 2nd, 3rd Harmonic vs Input Frequency, –1dBFS, 65Msps, 2V Range



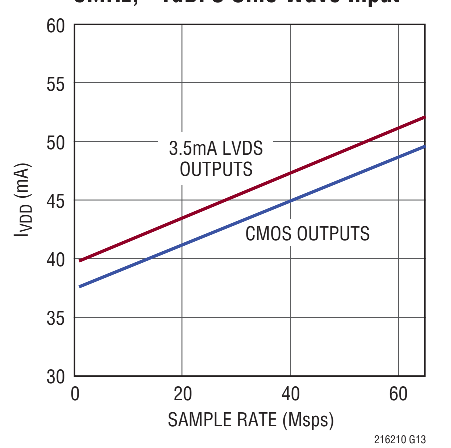
LTC2162: 2nd, 3rd Harmonic vs Input Frequency, –1dBFS, 65Msps, 1V Range



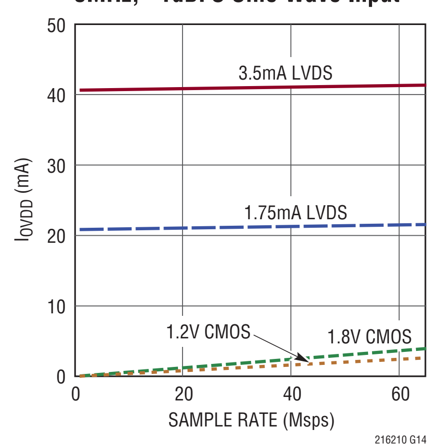
LTC2162: SFDR vs Input Level, f_{IN} = 70MHz, 65Msps, 2V Range



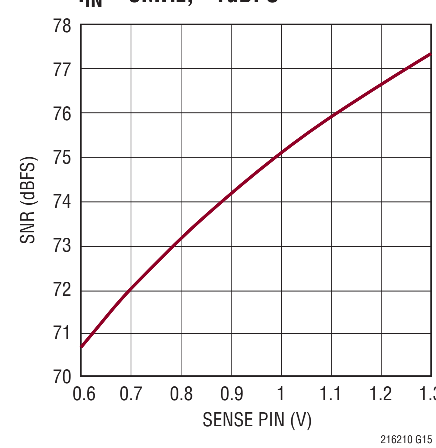
LTC2162: I_{VDD} vs Sample Rate, 5MHz, –1dBFS Sine Wave Input



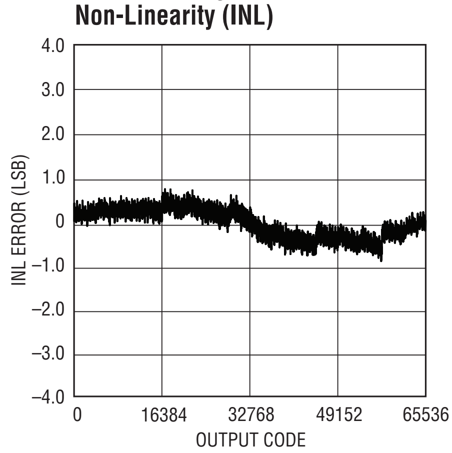
LTC2162: I_{OVDD} vs Sample Rate, 5MHz, –1dBFS Sine Wave Input



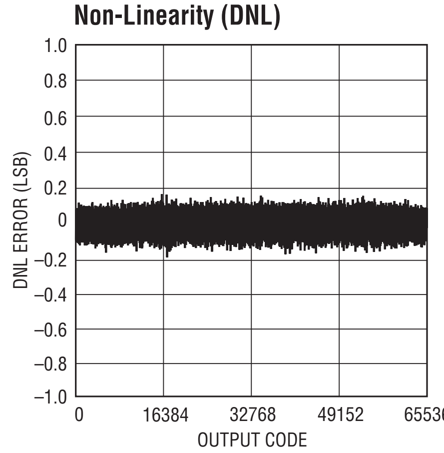
LTC2162: SNR vs SENSE, f_{IN} = 5MHz, –1dBFS



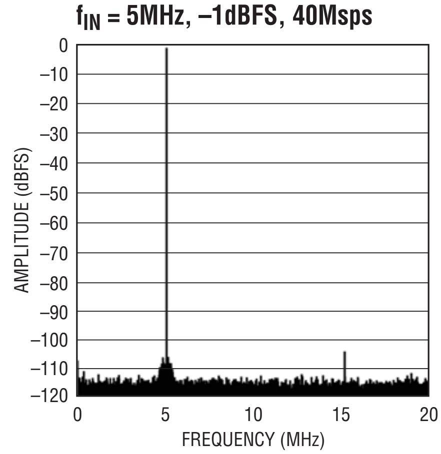
LTC2161: Integral Non-Linearity (INL)



LTC2161: Differential Non-Linearity (DNL)

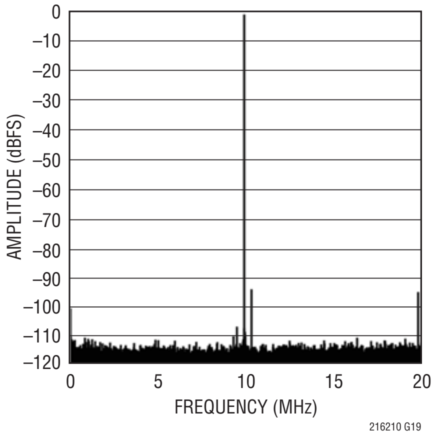


LTC2161: 64k Point FFT, f_{IN} = 5MHz, –1dBFS, 40Msps

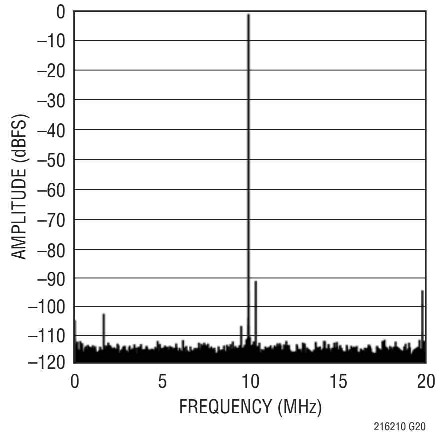


TYPICAL PERFORMANCE CHARACTERISTICS

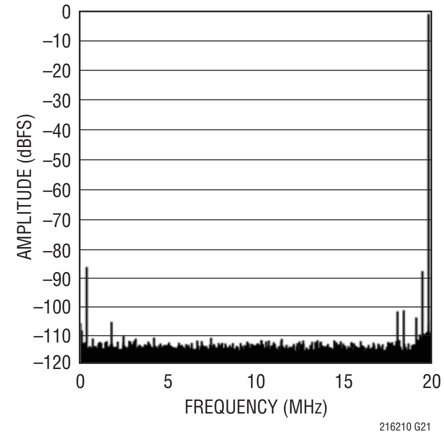
LTC2161: 64k Point FFT, f_{IN} = 30MHz, –1dBFS, 40Msps



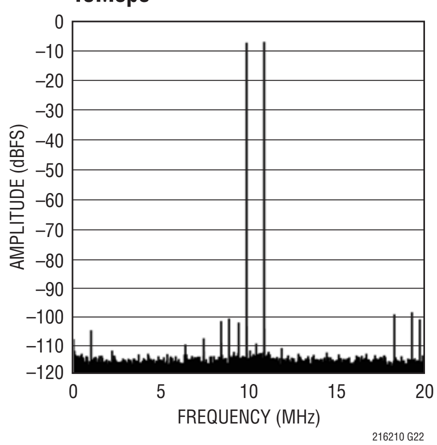
LTC2161: 64k Point FFT, f_{IN} = 70MHz, –1dBFS, 40Msps



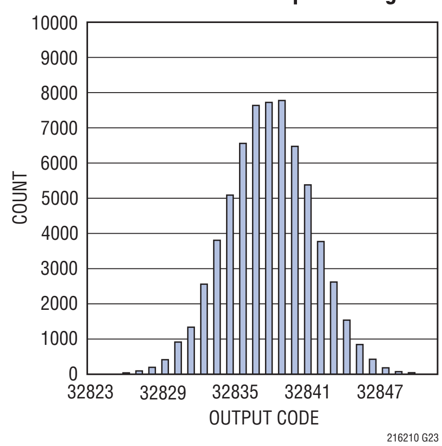
LTC2161: 64k Point FFT, f_{IN} = 140MHz, –1dBFS, 40Msps



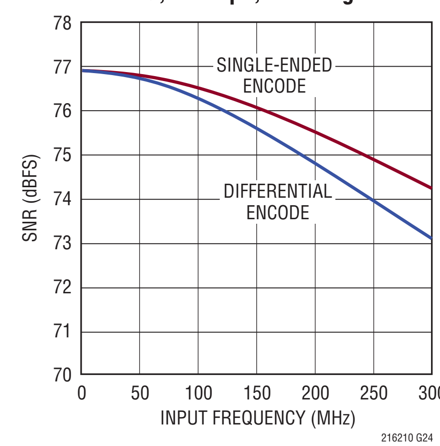
LTC2161: 64k Point 2-Tone FFT, f_{IN} = 69MHz, 70MHz, –7dBFS, 40Msps



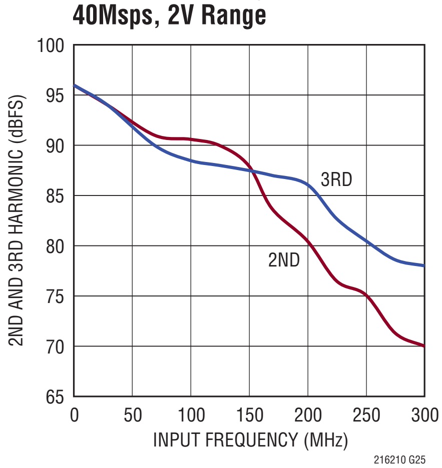
LTC2161: Shorted Input Histogram



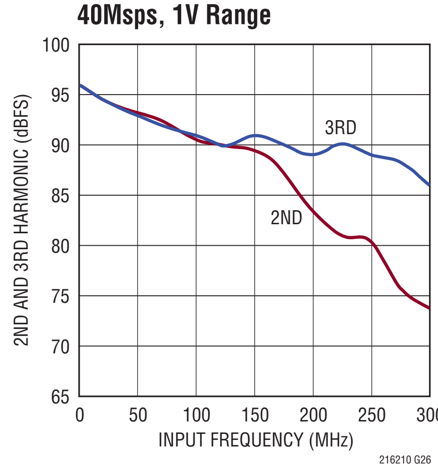
LTC2161: SNR vs Input Frequency, –1dBFS, 40Msps, 2V Range



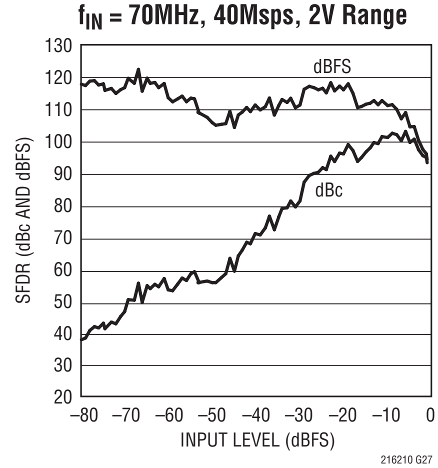
LTC2161: 2nd, 3rd Harmonic vs Input Frequency, –1dBFS, 40Msps, 2V Range



LTC2161: 2nd, 3rd Harmonic vs Input Frequency, –1dBFS, 40Msps, 1V Range

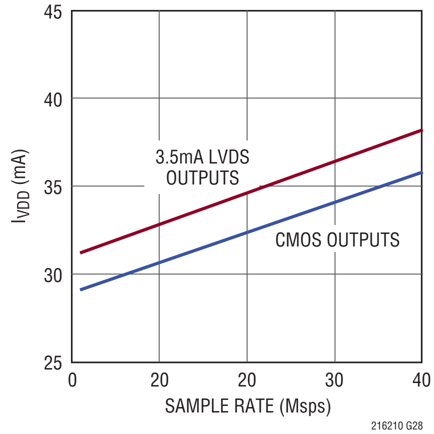


LTC2161: SFDR vs Input Level, f_{IN} = 70MHz, 40Msps, 2V Range

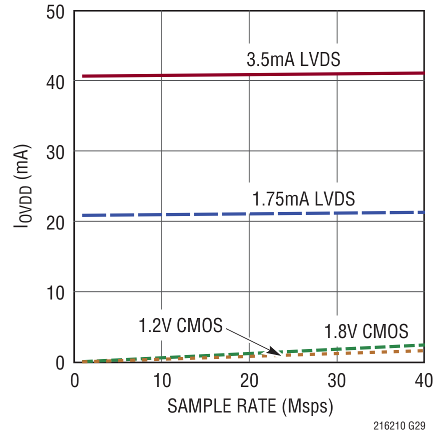


TYPICAL PERFORMANCE CHARACTERISTICS

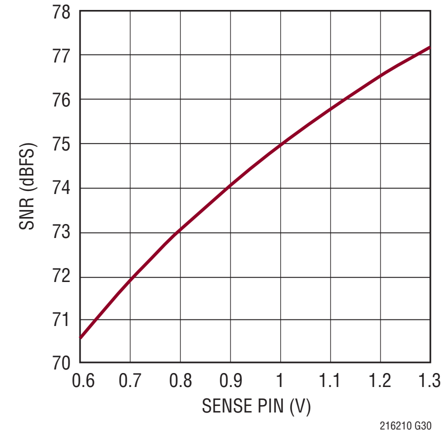
LTC2161: I_{VDD} vs Sample Rate, 5MHz, –1dBFS Sine Wave Input



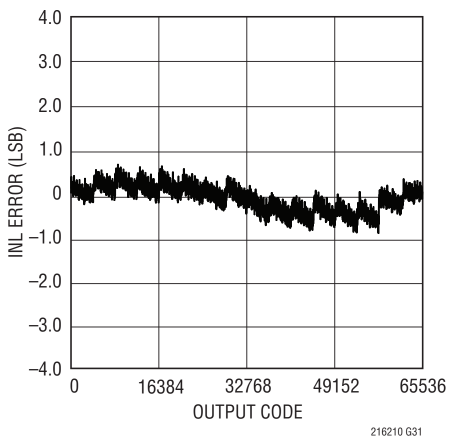
LTC2161: I_{OVDD} vs Sample Rate, 5MHz, –1dBFS Sine Wave Input



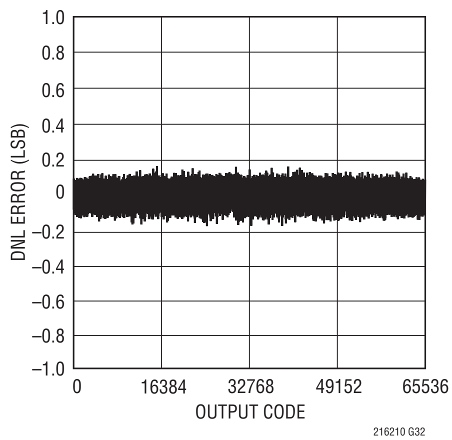
LTC2161: SNR vs SENSE, f_{IN} = 5MHz, –1dBFS



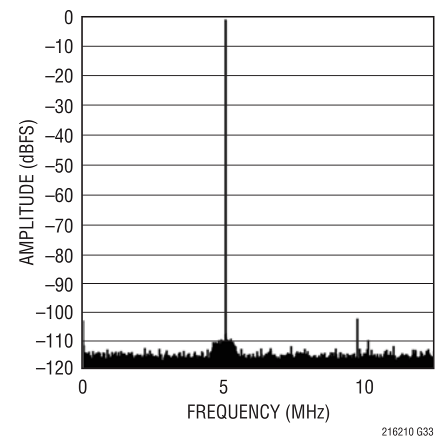
LTC2160: Integral Non-Linearity (INL)



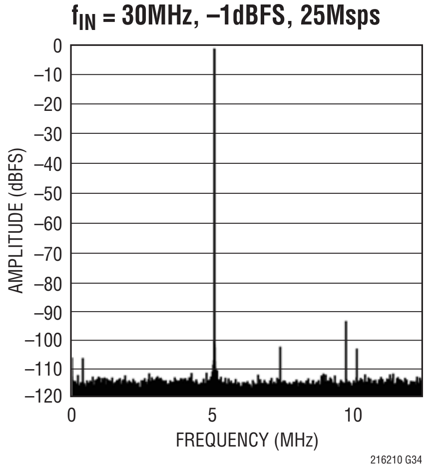
LTC2160: Differential Non-Linearity (DNL)



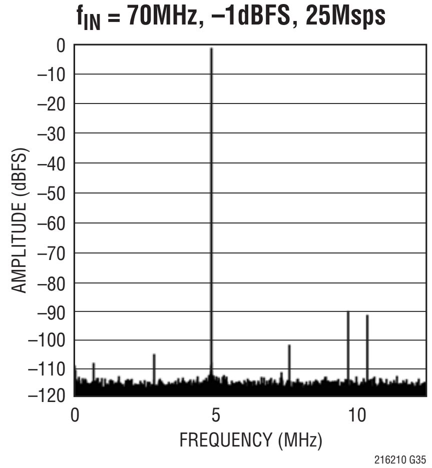
LTC2160: 64k Point FFT, f_{IN} = 5MHz, –1dBFS, 25Msps



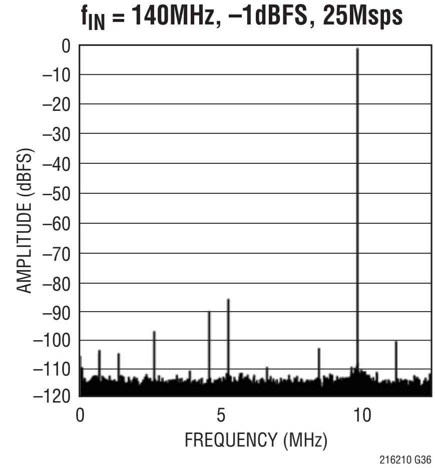
LTC2160: 64k Point FFT, f_{IN} = 30MHz, –1dBFS, 25Msps



LTC2160: 64k Point FFT, f_{IN} = 70MHz, –1dBFS, 25Msps

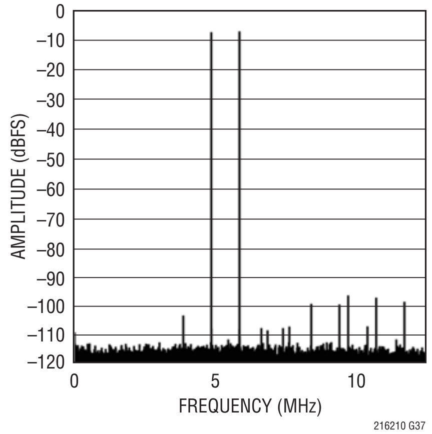


LTC2160: 64k Point FFT, f_{IN} = 140MHz, –1dBFS, 25Msps

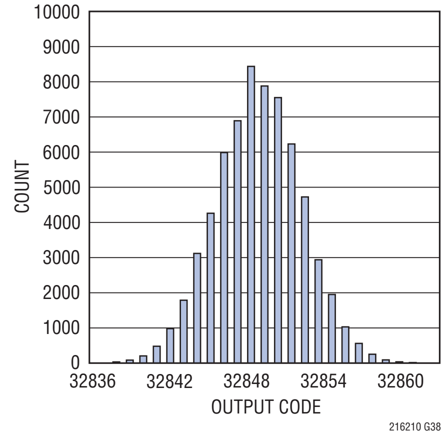


TYPICAL PERFORMANCE CHARACTERISTICS

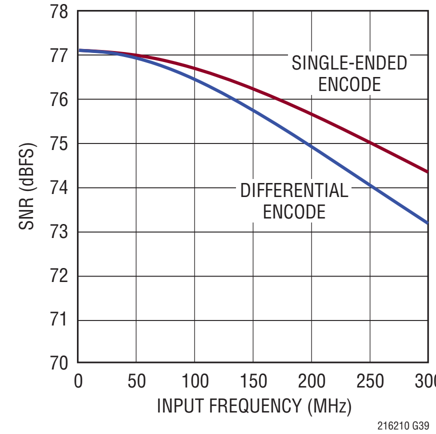
LTC2160: 64k Point 2-Tone FFT, f_{IN} = 69MHz, 70MHz, –7dBFS, 25Msps



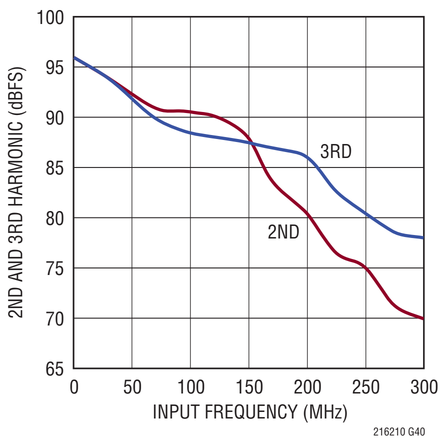
LTC2160: Shorted Input Histogram



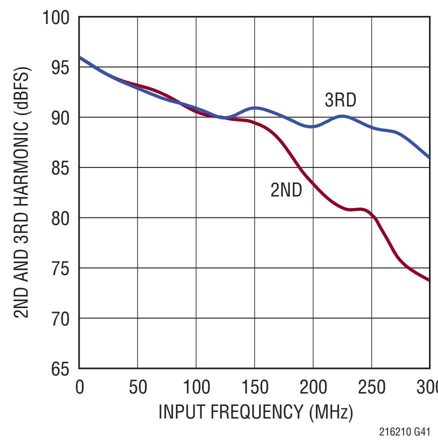
LTC2160: SNR vs Input Frequency, –1dBFS, 25Msps, 2V Range



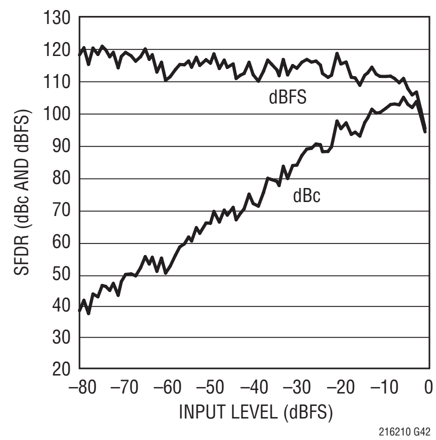
LTC2160: 2nd, 3rd Harmonic vs Input Frequency, –1dBFS, 25Msps, 2V Range



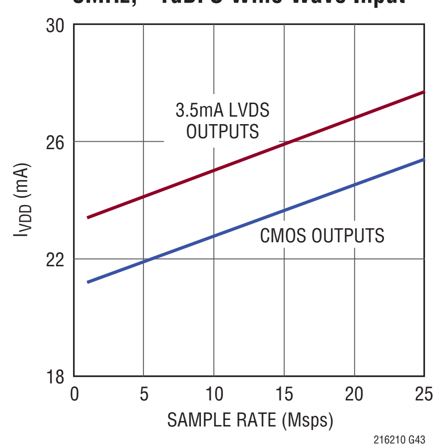
LTC2160: 2nd, 3rd Harmonic vs Input Frequency, –1dBFS, 25Msps, 1V Range



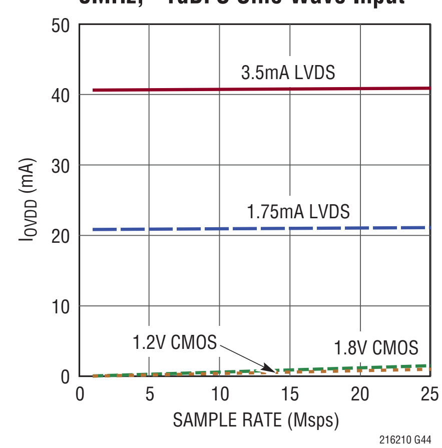
LTC2160: SFDR vs Input Level, f_{IN} = 70MHz, 25Msps, 2V Range



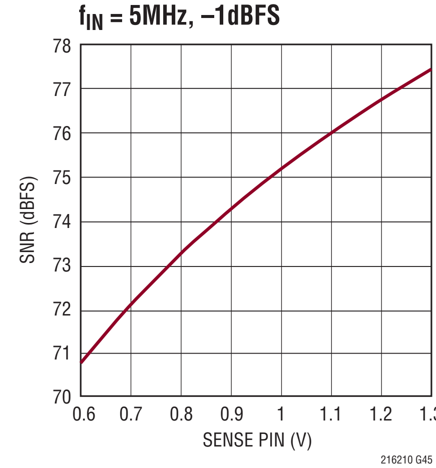
LTC2160: I_{VDD} vs Sample Rate, 5MHz, –1dBFS Wine Wave Input



LTC2160: I_{OVDD} vs Sample Rate, 5MHz, –1dBFS Sine Wave Input



LTC2160: SNR vs SENSE, f_{IN} = 5MHz, –1dBFS



PIN FUNCTIONS

(Pins that are the Same for All Digital Output Modes)

V_{CM} (Pin 1): Common Mode Bias Output. Nominally equal to $V_{DD}/2$. V_{CM} should be used to bias the common mode of the analog inputs. Bypass to ground with a 0.1µF ceramic capacitor.

A_{IN}^+ (Pin 2): Positive Differential Analog Input.

A_{IN}^- (Pin 3): Negative Differential Analog Input.

GND (Pins 4, 10, 11, 14, 20, 43, Exposed Pad Pin 49): ADC Power Ground. The exposed pad must be soldered to the PCB ground.

REFH (Pins 5, 7): ADC High Reference. See the Applications Information section for recommended bypassing circuits for REFH and REFL.

REFL (Pins 6, 8): ADC Low Reference. See the Applications Information section for recommended bypassing circuits for REFH and REFL.

PAR/$\overline{\text{SER}}$ (Pin 9): Programming Mode Selection Pin. Connect to ground to enable the serial programming mode. $\overline{\text{CS}}$, SCK, SDI, SDO become a serial interface that control the A/D operating modes. Connect to V_{DD} to enable the parallel programming mode where $\overline{\text{CS}}$, SCK, SDI, SDO become parallel logic inputs that control a reduced set of the A/D operating modes. PAR/$\overline{\text{SER}}$ should be connected directly to ground or V_{DD} and not be driven by a logic signal.

V_{DD} (Pins 12, 13, 47, 48): Analog Power Supply, 1.7V to 1.9V. Bypass to ground with 0.1µF ceramic capacitors. Adjacent pins can share a bypass capacitor.

ENC$^+$ (Pin 15): Encode Input. Conversion starts on the rising edge.

ENC$^-$ (Pin 16): Encode Complement Input. Conversion starts on the falling edge. Tie to GND for single-ended encode mode.

$\overline{\text{CS}}$ (Pin 17): Serial Interface Chip Select Input. In serial programming mode (PAR/$\overline{\text{SER}}$ = 0V), $\overline{\text{CS}}$ is the serial interface chip select input. When $\overline{\text{CS}}$ is low, SCK is enabled for shifting data on SDI into the mode control registers. In the parallel programming mode (PAR/$\overline{\text{SER}}$ = V_{DD}), $\overline{\text{CS}}$ controls the clock duty cycle stabilizer (see Table 2). $\overline{\text{CS}}$ can be driven with 1.8V to 3.3V logic.

SCK (Pin 18): Serial Interface Clock Input. In serial programming mode, (PAR/$\overline{\text{SER}}$ = 0V), SCK is the serial interface clock input. In the parallel programming mode (PAR/$\overline{\text{SER}}$ = V_{DD}), SCK controls the digital output mode (see Table 2). SCK can be driven with 1.8V to 3.3V logic.

SDI (Pin 19): Serial Interface Data Input. In serial programming mode, (PAR/$\overline{\text{SER}}$ = 0V), SDI is the serial interface data input. Data on SDI is clocked into the mode control registers on the rising edge of SCK. In the parallel programming mode (PAR/$\overline{\text{SER}}$ = V_{DD}), SDI can be used together with SDO to power down the part (Table 2). SDI can be driven with 1.8V to 3.3V logic.

OGND (Pin 31): Output Driver Ground. Must be shorted to the ground plane by a very low inductance path. Use multiple vias close to the pin.

OV_{DD} (Pin 32): Output Driver Supply. Bypass to ground with a 0.1µF ceramic capacitor.

SDO (Pin 44): Serial Interface Data Output. In serial programming mode, (PAR/$\overline{\text{SER}}$ = 0V), SDO is the optional serial interface data output. Data on SDO is read back from the mode control registers and can be latched on the falling edge of SCK. SDO is an open-drain NMOS output that requires an external 2k pull-up resistor to 1.8V – 3.3V. If read back from the mode control registers is not needed, the pull-up resistor is not necessary and SDO can be left unconnected. In the parallel programming mode (PAR/$\overline{\text{SER}}$ = V_{DD}), SDO can be used together with SDI to power down the part (Table 2). When used as an input, SDO can be driven with 1.8V to 3.3V logic through a 1k series resistor.

V_{REF} (Pin 45): Reference Voltage Output. Bypass to ground with a 2.2µF ceramic capacitor. The output voltage is nominally 1.25V.

SENSE (Pin 46): Reference Programming Pin. Connecting SENSE to V_{DD} selects the internal reference and a ±1V input range. Connecting SENSE to ground selects the internal reference and a ±0.5V input range. An external reference between 0.625V and 1.3V applied to SENSE selects an input range of $\pm 0.8 \bullet V_{SENSE}$.

PIN FUNCTIONS

FULL RATE CMOS OUTPUT MODE

All Pins Below Have CMOS Output Levels (OGND to O_{VDD})

D0 to D15 (Pins 21-28, 33-40): Digital Outputs. D15 is the MSB.

CLKOUT$^-$ (Pin 29): Inverted version of CLKOUT$^+$.

CLKOUT$^+$ (Pin 30): Data Output Clock. The digital outputs normally transition at the same time as the falling edge of CLKOUT$^+$. The phase of CLKOUT$^+$ can also be delayed relative to the digital outputs by programming the mode control registers.

DNC (Pin 41): Do not connect this pin.

OF (Pin 42): Overflow/Underflow Digital Output. OF is high when an overflow or underflow has occurred.

DOUBLE DATA RATE CMOS OUTPUT MODE

All Pins Below Have CMOS Output Levels (OGND to O_{VDD})

D0_1 to D14_15 (Pins 22, 24, 26, 28, 34, 36, 38, 40): Double Data Rate Digital Outputs. Two data bits are multiplexed onto each output pin. The even data bits (D0, D2, D4, D6, D8, D10, D12, D14) appear when CLKOUT$^+$ is low. The odd data bits (D1, D3, D5, D7, D9, D11, D13, D15) appear when CLKOUT$^+$ is high.

DNC (Pins 21, 23, 25, 27, 33, 35, 37, 39, 41): Do not connect these pins.

CLKOUT$^-$ (Pin 29): Inverted version of CLKOUT$^+$.

CLKOUT$^+$ (Pin 30): Data Output Clock. The digital outputs normally transition at the same time as the falling and rising edges of CLKOUT$^+$. The phase of CLKOUT$^+$ can also be delayed relative to the digital outputs by programming the mode control registers.

OF (Pin 42): Overflow/Underflow Digital Output. OF is high when an overflow or underflow has occurred.

DOUBLE DATA RATE LVDS OUTPUT MODE

All Pins Below Have LVDS Output Levels. The Output Current Level is Programmable. There is an Optional Internal 100Ω Termination Resistor Between the Pins of Each LVDS Output Pair.

D0_1$^-$/D0_1$^+$ to D14_15$^-$/D14_15$^+$ (Pins 21/22, 23/24, 25/26, 27/28, 33/34, 35/36, 37/38, 39/40): Double Data Rate Digital Outputs. Two data bits are multiplexed onto each differential output pair. The even data bits (D0, D2, D4, D6, D8, D10, D12, D14) appear when CLKOUT$^+$ is low. The odd data bits (D1, D3, D5, D7, D9, D11, D13, D15) appear when CLKOUT$^+$ is high.

CLKOUT$^-$/CLKOUT$^+$ (Pins 39/40): Data Output Clock. The digital outputs normally transition at the same time as the falling and rising edges of CLKOUT$^+$. The phase of CLKOUT$^+$ can also be delayed relative to the digital outputs by programming the mode control registers.

OF$^-$/OF$^+$ (Pins 41/42): Overflow/Underflow Digital Output. OF$^+$ is high when an overflow or underflow has occurred.

FUNCTIONAL BLOCK DIAGRAM

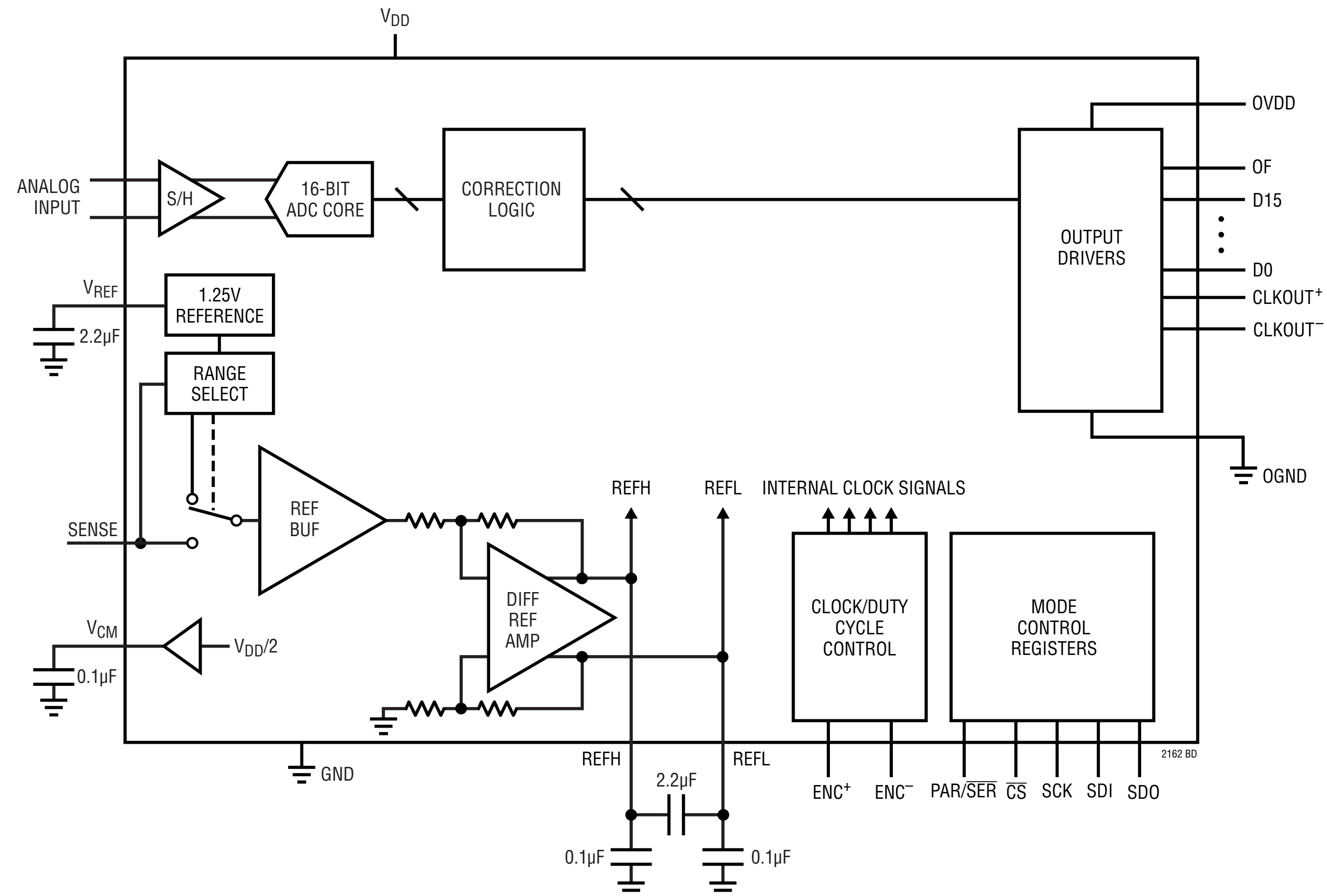


Figure 1. Functional Block Diagram

APPLICATIONS INFORMATION

CONVERTER OPERATION

The LTC2162/LTC2161/LTC2160 are low power, 16-bit, 65Msps/40Msps/25Msps A/D converters that are powered by a single 1.8V supply. The analog inputs should be driven differentially. The encode input can be driven differentially or single-ended for lower power consumption. The digital outputs can be CMOS, double data rate CMOS (to halve the number of output lines), or double data rate LVDS (to reduce digital noise in the system). Many additional features can be chosen by programming the mode control registers through a serial SPI port.

ANALOG INPUT

The analog inputs are differential CMOS sample-and-hold circuits (Figure 2). The inputs should be driven differentially around a common mode voltage set by the V_{CM} output pin, which is nominally $V_{DD}/2$. For the 2V input range, the inputs should swing from V_{CM} – 0.5V to V_{CM} + 0.5V. There should be 180° phase difference between the inputs.

APPLICATIONS INFORMATION

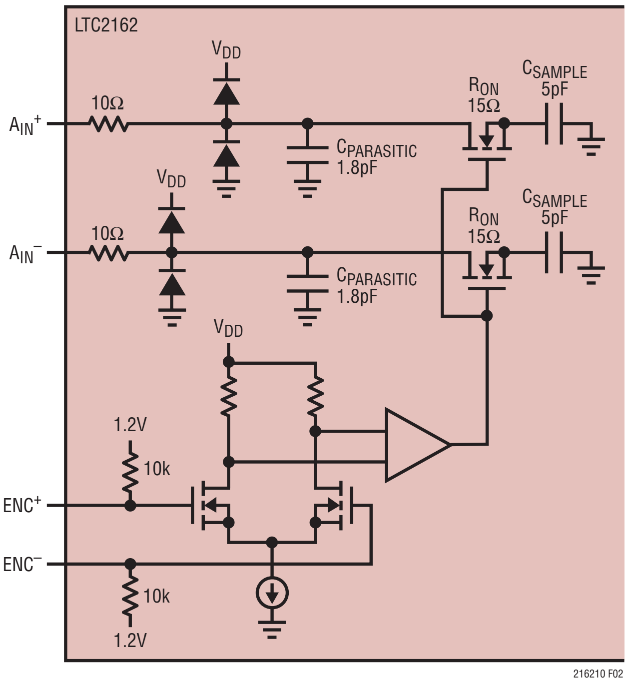


Figure 2. Equivalent Input Circuit

Single-Ended Input

For applications less sensitive to harmonic distortion, the A_{IN}^+ input can be driven single-ended with a $1V_{P-P}$ signal centered around V_{CM}. The A_{IN}^- input should be connected to V_{CM} and the V_{CM} bypass capacitor should be increased to 2.2µF. With a single-ended input the harmonic distortion and INL will degrade, but the noise and DNL will remain unchanged.

INPUT DRIVE CIRCUITS

Input filtering

If possible, there should be an RC lowpass filter right at the analog inputs. This lowpass filter isolates the drive circuitry from the A/D sample-and-hold switching, and also limits wideband noise from the drive circuitry. Figure 3 shows an example of an input RC filter. The RC component values should be chosen based on the application's input frequency.

Transformer Coupled Circuits

Figure 3 shows the analog input being driven by an RF transformer with a center-tapped secondary. The center tap is biased with V_{CM}, setting the A/D input at its optimal DC level. At higher input frequencies a transmission line balun transformer (Figures 4 through 6) has better balance, resulting in lower A/D distortion.

Amplifier Circuits

Figure 7 shows the analog input being driven by a high speed differential amplifier. The output of the amplifier is AC coupled to the A/D so the amplifier's output common mode voltage can be optimally set to minimize distortion.

At very high frequencies an RF gain block will often have lower distortion than a differential amplifier. If the gain block is single-ended, then a transformer circuit (Figures 4 through 6) should convert the signal to differential before driving the A/D.

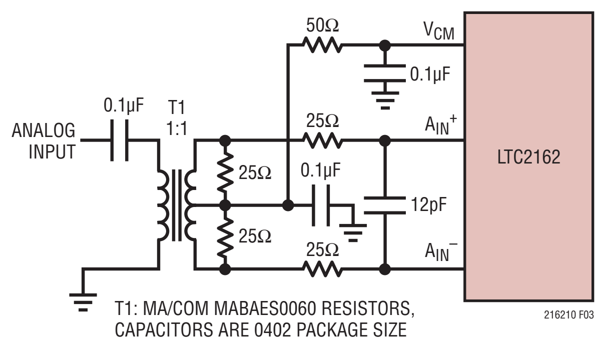
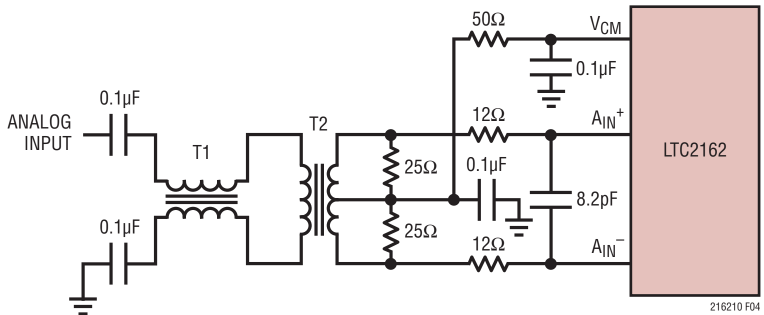


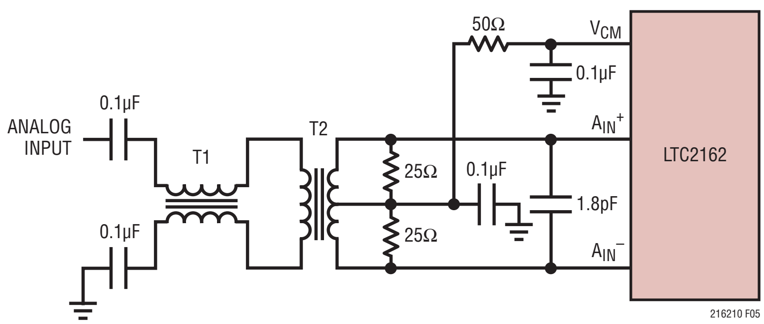
Figure 3. Analog Input Circuit Using a Transformer. Recommended for Input Frequencies from 5MHz to 70MHz

APPLICATIONS INFORMATION



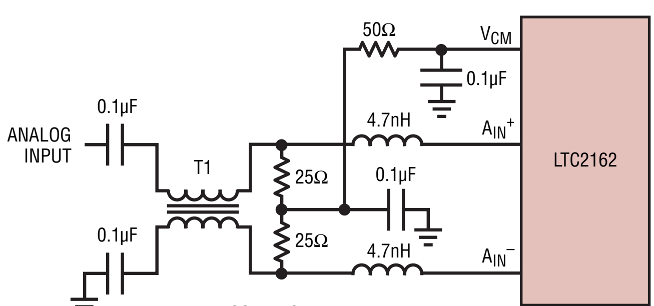
T1: MA/COM MABA-007159-000000
T2: COILCRAFT WBC1-1TL
RESISTORS, CAPACITORS ARE 0402 PACKAGE SIZE

Figure 4. Recommended Front End Circuit for Input Frequencies from 5MHz to 150MHz



T1: MA/COM MABA-007159-000000
T2: COILCRAFT WBC1-1TL
RESISTORS, CAPACITORS ARE 0402 PACKAGE SIZE

Figure 5. Recommended Front End Circuit for Input Frequencies from 150MHz to 250MHz



T1: MA/COM ETC1-1-13
RESISTORS, CAPACITORS
ARE 0402 PACKAGE SIZE

Figure 6. Recommended Front End Circuit for Input Frequencies Above 250MHz

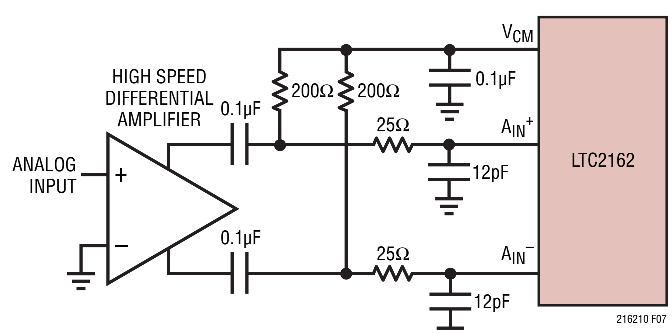


Figure 7. Front End Circuit Using a High Speed Differential Amplifier

APPLICATIONS INFORMATION

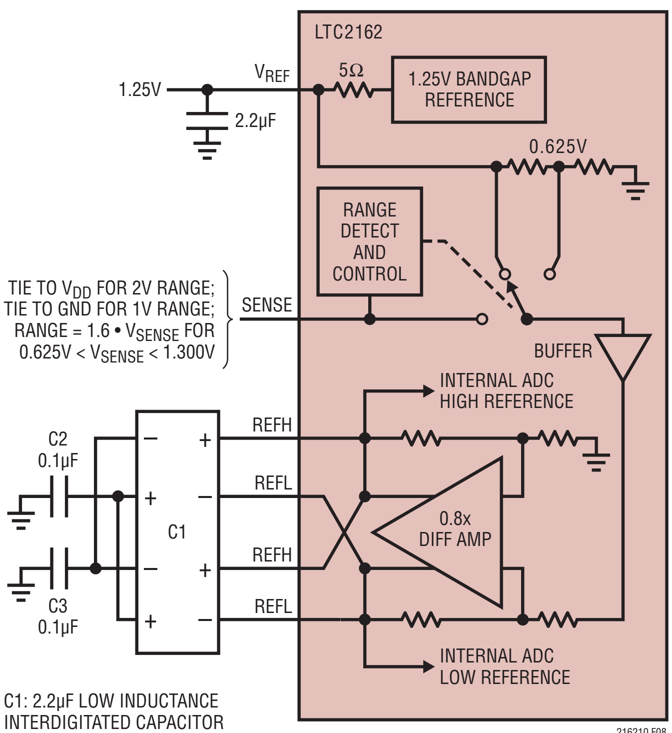
Reference

The LTC2162/LTC2161/LTC2160 has an internal 1.25V voltage reference. For a 2V input range using the internal reference, connect SENSE to V_{DD}. For a 1V input range using the internal reference, connect SENSE to ground. For a 2V input range with an external reference, apply a 1.25V reference voltage to SENSE (Figure 9).

The input range can be adjusted by applying a voltage to SENSE that is between 0.625V and 1.30V. The input range will then be $1.6 \bullet V_{SENSE}$.

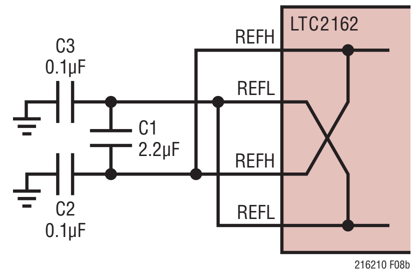
The V_{REF}, REFH and REFL pins should be bypassed as shown in Figure 8a. A low inductance 2.2µF interdigitated capacitor is recommended for the bypass between REFH and REFL. This type of capacitor is available at a low cost from multiple suppliers.

Alternatively, C1 can be replaced by a standard 2.2µF capacitor between REFH and REFL. The capacitor should be as close to the pins as possible (not on the back side of the circuit board).



C1: 2.2µF LOW INDUCTANCE
INTERDIGITATED CAPACITOR
TDK CLLE1AX7S0G225M
MURATA LLA219C70G225M
AVX W2L14Z225M
OR EQUIVALENT

Figure 8a. Reference Circuit



CAPACITORS ARE 0402 PACKAGE SIZE

Figure 8b. Alternative REFH/REFL Bypass Circuit

Figures 8c and 8d show the recommended circuit board layout for the REFH/REFL bypass capacitors. Note that in Figure 8c, every pin of the interdigitated capacitor (C1) is connected since the pins are not internally connected in some vendors' capacitors. In Figure 8d, the REFH and REFL pins are connected by short jumpers in an internal layer. To minimize the inductance of these jumpers they can be placed in a small hole in the GND plane on the second board layer.

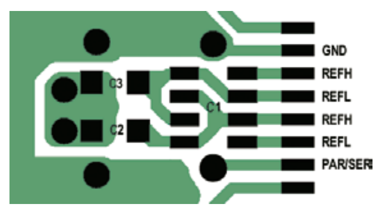


Figure 8c. Recommended Layout for the REFH/REFL Bypass Circuit in Figure 8a

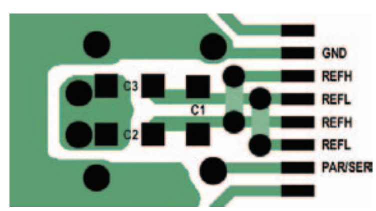


Figure 8d. Recommended Layout for the REFH/REFL Bypass Circuit in Figure 8b

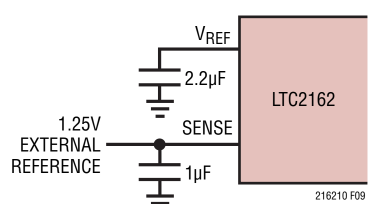


Figure 9. Using an External 1.25V Reference

APPLICATIONS INFORMATION

Encode Input

The signal quality of the encode inputs strongly affects the A/D noise performance. The encode inputs should be treated as analog signals—do not route them next to digital traces on the circuit board. There are two modes of operation for the encode inputs: the differential encode mode (Figure 10), and the single-ended encode mode (Figure 11).

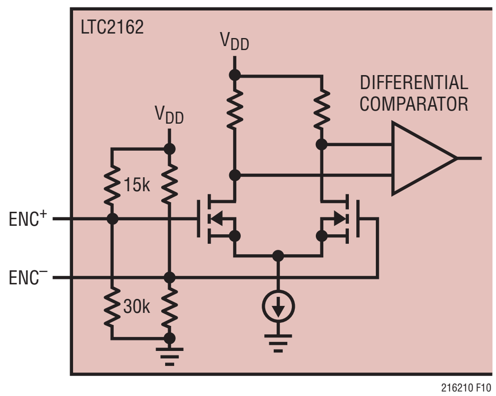


Figure 10. Equivalent Encode Input Circuit for Differential Encode Mode

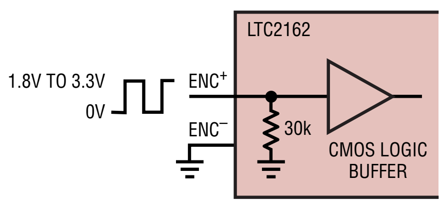
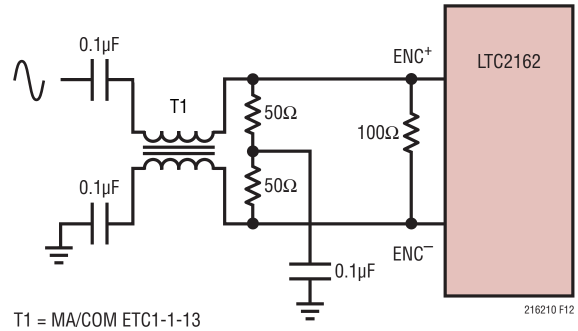


Figure 11. Equivalent Encode Input Circuit for Single-Ended Encode Mode.

The differential encode mode is recommended for sinusoidal, PECL, or LVDS encode inputs (Figures 12, 13). The encode inputs are internally biased to 1.2V through 10kΩ equivalent resistance. The encode inputs can be taken above V_{DD} (up to 3.6V), and the common mode range is from 1.1V to 1.6V. In the differential encode mode, ENC^- should stay at least 200mV above ground to avoid falsely triggering the single-ended encode mode. For good jitter performance ENC^+ and ENC^- should have fast rise and fall times.

The single ended encode mode should be used with CMOS encode inputs. To select this mode, ENC^- is connected to ground and ENC^+ is driven with a square wave encode input. ENC^+ can be taken above V_{DD} (up to 3.6V) enabling 1.8V to 3.3V CMOS logic levels to be used. The ENC^+ threshold is 0.9V. For good jitter performance ENC^+ should have fast rise and fall times.



T1 = MA/COM ETC1-1-13
RESISTORS AND CAPACITORS
ARE 0402 PACKAGE SIZE

Figure 12. Sinusoidal Encode Drive

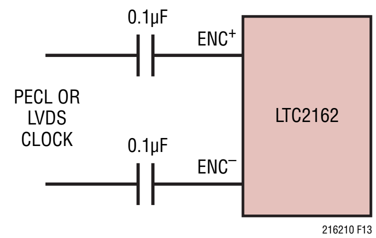


Figure 13. PECL or LVDS Encode Drive

If the encode signal is turned off or drops below approximately 500kHz, the A/D enters nap mode.

Clock Duty Cycle Stabilizer

For good performance the encode signal should have a 50%(±5%) duty cycle. If the optional clock duty cycle stabilizer circuit is enabled, the encode duty cycle can vary from 30% to 70% and the duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the encode signal changes frequency, the duty cycle stabilizer circuit requires one hundred clock cycles to lock onto the input clock. The duty cycle stabilizer is enabled by mode control register A2 (serial programming mode), or by $\overline{CS}$ (parallel programming mode).

For applications where the sample rate needs to be changed quickly, the clock duty cycle stabilizer can be disabled. If the duty cycle stabilizer is disabled, care should be taken to make the sampling clock have a 50%(±5%) duty cycle. The duty cycle stabilizer should not be used below 5Msps.

APPLICATIONS INFORMATION

DIGITAL OUTPUTS

Digital Output Modes

The LTC2162/LTC2161/LTC2160 can operate in three digital output modes: full rate CMOS, double data rate CMOS (to halve the number of output lines), or double data rate LVDS (to reduce digital noise in the system.) The output mode is set by mode control register A3 (serial programming mode), or by SCK (parallel programming mode). Note that double data rate CMOS cannot be selected in the parallel programming mode.

Full Rate CMOS Mode

In full rate CMOS mode the data outputs (D0 to D15), overflow (OF), and the data output clocks ($CLKOUT^+$, $CLKOUT^–$) have CMOS output levels. The outputs are powered by OV_{DD} and OGND which are isolated from the A/D core power and ground. OV_{DD} can range from 1.1V to 1.9V, allowing 1.2V through 1.8V CMOS logic outputs.

For good performance, the digital outputs should drive minimal capacitive loads. If the load capacitance is larger than 10pF, a digital buffer should be used.

Double Data Rate CMOS Mode

In double data rate CMOS mode, two data bits are multiplexed and output on each data pin. This reduces the number of digital lines by eight, simplifying board routing and reducing the number of input pins needed to receive the data. The data outputs (D0_1, D2_3, D4_5, D6_7, D8_9, D10_11, D12_13, D14_15), overflow (OF), and the data output clocks ($CLKOUT^+$, $CLKOUT^–$) have CMOS output levels. The outputs are powered by OV_{DD} and OGND which are isolated from the A/D core power and ground. OV_{DD} can range from 1.1V to 1.9V, allowing 1.2V through 1.8V CMOS logic outputs.

For good performance, the digital outputs should drive minimal capacitive loads. If the load capacitance is larger than 10pF, a digital buffer should be used.

Double Data Rate LVDS Mode

In double data rate LVDS mode, two data bits are multiplexed and output on each differential output pair. There are eight LVDS output pairs ($D0\_1^+/D0\_1^–$ through $D14\_15^+/D14\_15^–$) for the digital output data. Overflow ($OF^+/OF^–$) and the data output clock ($CLKOUT^+/CLKOUT^–$) each have an LVDS output pair.

By default the outputs are standard LVDS levels: 3.5mA output current and a 1.25V output common mode voltage. An external 100Ω differential termination resistor is required for each LVDS output pair. The termination resistors should be located as close as possible to the LVDS receiver.

The outputs are powered by OV_{DD} and OGND which are isolated from the A/D core power and ground. In LVDS mode, OV_{DD} must be 1.8V.

Programmable LVDS Output Current

In LVDS mode, the default output driver current is 3.5mA. This current can be adjusted by serially programming mode control register A3. Available current levels are 1.75mA, 2.1mA, 2.5mA, 3mA, 3.5mA, 4mA and 4.5mA.

Optional LVDS Driver Internal Termination

In most cases using just an external 100Ω termination resistor will give excellent LVDS signal integrity. In addition, an optional internal 100Ω termination resistor can be enabled by serially programming mode control register A3. The internal termination helps absorb any reflections caused by imperfect termination at the receiver. When the internal termination is enabled, the output driver current is doubled to maintain the same output voltage swing.

Overflow Bit

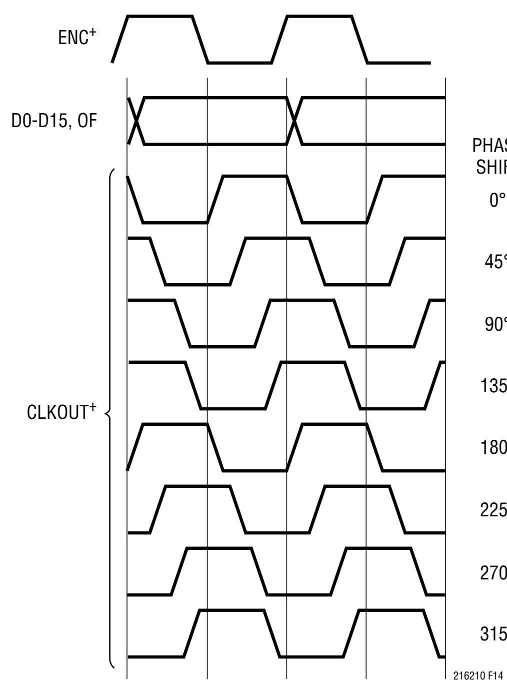
The overflow output bit outputs a logic high when the analog input is either overranged or underranged. The overflow bit has the same pipeline latency as the data bits.

APPLICATIONS INFORMATION

Phase-Shifting the Output Clock

In full rate CMOS mode the data output bits normally change at the same time as the falling edge of CLKOUT+, so the rising edge of CLKOUT+ can be used to latch the output data. In double data rate CMOS and LVDS modes the data output bits normally change at the same time as the falling and rising edges of CLKOUT+. To allow adequate setup and hold time when latching the data, the CLKOUT+ signal may need to be phase-shifted relative to the data output bits. Most FPGAs have this feature; this is generally the best place to adjust the timing.

The LTC2162/LTC2161/LTC2160 can also phase-shift the CLKOUT+/CLKOUT– signals by serially programming mode control register A2. The output clock can be shifted by 0°, 45°, 90°, or 135°. To use the phase-shifting feature the clock duty cycle stabilizer must be turned on. Another control register bit can invert the polarity of CLKOUT+ and CLKOUT–, independently of the phase-shift. The combination of these two features enables phase-shifts of 45° up to 315° (Figure 14).



PHASE SHIFT	MODE CONTROL BITS CLKINV	CLKPHASE1	CLKPHASE0
0°	0	0	0
45°	0	0	1
90°	0	1	0
135°	0	1	1
180°	1	0	0
225°	1	0	1
270°	1	1	0
315°	1	1	1

Figure 14. Phase-Shifting CLKOUT

Table 1. Output Codes vs Input Voltage

$A_{IN}^+ - A_{IN}^-$ (2V RANGE)	OF	D15 – D0 (OFFSET BINARY)	D15 – D0 (2'S COMPLEMENT)
>1.000000V	1	1111 1111 1111 1111	0111 1111 1111 1111
+0.999970V	0	1111 1111 1111 1111	0111 1111 1111 1111
+0.999939V	0	1111 1111 1111 1110	0111 1111 1111 1110
+0.000030V	0	1000 0000 0000 0001	0000 0000 0000 0001
+0.000000V	0	1000 0000 0000 0000	0000 0000 0000 0000
–0.000030V	0	0111 1111 1111 1111	1111 1111 1111 1111
–0.000061V	0	0111 1111 1111 1110	1111 1111 1111 1110
–0.999939V	0	0000 0000 0000 0001	1000 0000 0000 0001
–1.000000V	0	0000 0000 0000 0000	1000 0000 0000 0000
< –1.000000V	1	0000 0000 0000 0000	1000 0000 0000 0000

APPLICATIONS INFORMATION

DATA FORMAT

Table 1 shows the relationship between the analog input voltage, the digital data output bits and the overflow bit. By default the output data format is offset binary. The 2's complement format can be selected by serially programming mode control register A4.

Digital Output Randomizer

Interference from the A/D digital outputs is sometimes unavoidable. Digital interference may be from capacitive or inductive coupling or coupling through the ground plane. Even a tiny coupling factor can cause unwanted tones in the ADC output spectrum. By randomizing the digital output before it is transmitted off chip, these unwanted tones can be randomized which reduces the unwanted tone amplitude.

The digital output is randomized by applying an exclusive-OR logic operation between the LSB and all other data output bits. To decode, the reverse operation is applied —an exclusive-OR operation is applied between the LSB and all other bits. The LSB, OF and CLKOUT outputs are not affected. The output randomizer is enabled by serially programming mode control register A4.

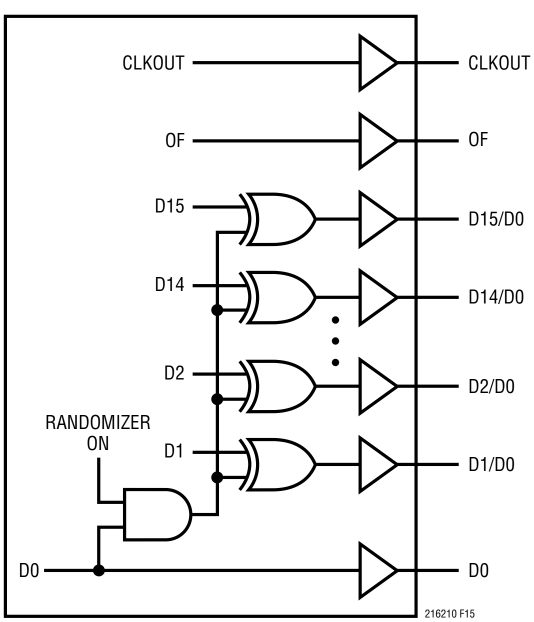


Figure 15. Functional Equivalent of Digital Output Randomizer

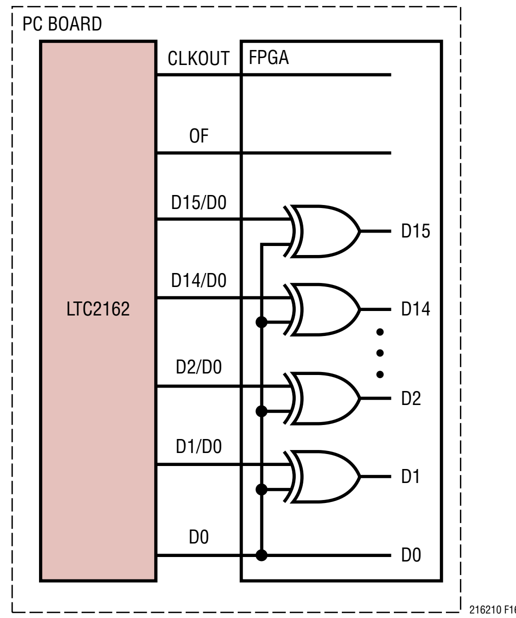


Figure 16. Unrandomizing a Randomized Digital Output Signal

Alternate Bit Polarity

Another feature that reduces digital feedback on the circuit board is the alternate bit polarity mode. When this mode is enabled, all of the odd bits (D1, D3, D5, D7, D9, D11, D13, D15) are inverted before the output buffers. The even bits (D0, D2, D4, D6, D8, D10, D12, D14), OF and CLKOUT are not affected. This can reduce digital currents in the circuit board ground plane and reduce digital noise, particularly for very small analog input signals.

When there is a very small signal at the input of the A/D that is centered around mid-scale, the digital outputs toggle between mostly 1's and mostly 0's. This simultaneous switching of most of the bits will cause large currents in the ground plane. By inverting every other bit, the alternate bit polarity mode makes half of the bits transition high while half of the bits transition low. This cancels current flow in the ground plane, reducing the digital noise.

The digital output is decoded at the receiver by inverting the odd bits (D1, D3, D5, D7, D9, D11, D13, D15.) The alternate bit polarity mode is independent of the digital output randomizer—either, both or neither function can be on at the same time. The alternate bit polarity mode is enabled by serially programming mode control register A4.

APPLICATIONS INFORMATION

Digital Output Test Patterns

To allow in-circuit testing of the digital interface to the A/D, there are several test modes that force the A/D data outputs (OF, D15 to D0) to known values:

All 1s: all outputs are 1

All 0s: all outputs are 0

Alternating: outputs change from all 1s to all 0s on alternating samples.

Checkerboard: outputs change from 1010101010101010l to 01010101010101010 on alternating samples.

The digital output test patterns are enabled by serially programming mode control register A4. When enabled, the test patterns override all other formatting modes: 2's complement, randomizer, alternate bit polarity.

Output Disable

The digital outputs may be disabled by serially programming mode control register A3. All digital outputs including OF and CLKOUT are disabled. The high-impedance disabled state is intended for in-circuit testing or long periods of inactivity—it is too slow to multiplex a data bus between multiple converters at full speed. When the outputs are disabled the ADC should be put into either sleep or nap mode.

Sleep and Nap Modes

The A/D may be placed in sleep or nap modes to conserve power. In sleep mode the entire device is powered down, resulting in 1mW power consumption. The amount of time required to recover from sleep mode depends on the size of the bypass capacitors on V_{REF}, REFH, and REFL. For the suggested values in Figure 8, the A/D will stabilize after 2ms.

In nap mode the A/D core is powered down while the internal reference circuits stay active, allowing faster wake-up than from sleep mode. Recovering from nap mode requires at least 100 clock cycles. If the application demands very accurate DC settling then an additional 50μs should be allowed so the on-chip references can settle from the slight temperature shift caused by the change in supply current as the A/D leaves nap mode.

Sleep mode and nap mode are enabled by mode control register A1 (serial programming mode), or by SDI and SDO (parallel programming mode).

DEVICE PROGRAMMING MODES

The operating modes of the LTC2162/LTC2161/LTC2160 can be programmed by either a parallel interface or a simple serial interface. The serial interface has more flexibility and can program all available modes. The parallel interface is more limited and can only program some of the more commonly used modes.

Parallel Programming Mode

To use the parallel programming mode, PAR/$\overline{SER}$ should be tied to V_{DD}. The $\overline{CS}$, SCK, SDI and SDO pins are binary logic inputs that set certain operating modes. These pins can be tied to V_{DD} or ground, or driven by 1.8V, 2.5V, or 3.3V CMOS logic. When used as an input, SDO should be driven through a 1kΩ series resistor. Table 2 shows the modes set by $\overline{CS}$, SCK, SDI and SDO.

Table 2. Parallel Programming Mode Control Bits (PAR/$\overline{SER}$ = V_{DD})

PIN	DESCRIPTION
$\overline{CS}$	**Clock Duty Cycle Stabilizer Control Bit** 0 = Clock Duty Cycle Stabilizer Off 1 = Clock Duty Cycle Stabilizer On
SCK	**Digital Output Mode Control Bit** 0 = Full Rate CMOS Output Mode 1 = Double Data Rate LVDS Output Mode (3.5mA LVDS Current, Internal Termination Off)
SDI/SDO	**Power-Down Control Bits** 00 = Normal Operation 01 = Not Used 10 = Nap Mode 11 = Sleep Mode (Entire Device Powered Down)

APPLICATIONS INFORMATION

Serial Programming Mode

To use the serial programming mode, PAR/$\overline{SER}$ should be tied to ground. The $\overline{CS}$, SCK, SDI and SDO pins become a serial interface that program the A/D mode control registers. Data is written to a register with a 16-bit serial word. Data can also be read back from a register to verify its contents.

Serial data transfer starts when $\overline{CS}$ is taken low. The data on the SDI pin is latched at the first 16 rising edges of SCK. Any SCK rising edges after the first 16 are ignored. The data transfer ends when $\overline{CS}$ is taken high again.

The first bit of the 16-bit input word is the R/$\overline{W}$ bit. The next seven bits are the address of the register (A6:A0). The final eight bits are the register data (D7:D0).

If the R/$\overline{W}$ bit is low, the serial data (D7:D0) will be written to the register set by the address bits (A6:A0). If the R/$\overline{W}$ bit is high, data in the register set by the address bits (A6:A0) will be read back on the SDO pin (see the Timing Diagrams). During a read back command the register is not updated and data on SDI is ignored.

The SDO pin is an open drain output that pulls to ground with a 200Ω impedance. If register data is read back through SDO, an external 2k pull-up resistor is required. If serial data is only written and read back is not needed, then SDO can be left floating and no pull-up resistor is needed.

Table 3 shows a map of the mode control registers.

Software Reset

If serial programming is used, the mode control registers should be programmed as soon as possible after the power supplies turn on and are stable. The first serial command must be a software reset which will reset all register data bits to logic 0. To perform a software reset, bit D7 in the reset register is written with a logic 1. After the reset SPI write command is complete, bit D7 is automatically set back to zero.

Table 3. Serial Programming Mode Register Map (PAR/$\overline{SER}$ = GND)

REGISTER A0: RESET REGISTER (ADDRESS 00h)

D7	D6	D5	D4	D3	D2	D1	D0
RESET	X	X	X	X	X	X	X

Bits 7 **RESET** Software Reset Bit

0 = Not Used

1 = Software Reset. All Mode Control Registers are reset to 00h. The ADC is momentarily placed in sleep mode.
This bit is automatically set back to zero at the end of the SPI write command.
The Reset register is write-only. Data read back from the reset register will be random.

Bits 6-0 Unused, Don't Care Bits

REGISTER A1: POWER DOWN REGISTER (ADDRESS 01h)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	PWROFF1	PWROFF0

Bits 7-2 Unused, Don't Care Bits

Bits 1-0 **PWROFF1: PWROFF0** Power Down Control Bits

00 = Normal Operation

01 = Not Used

10 = Nap Mode

11 = Sleep Mode

APPLICATIONS INFORMATION

REGISTER A2: TIMING REGISTER (ADDRESS 02h)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	CLKINV	CLKPHASE1	CLKPHASE0	DCS

Bits 7-4 Unused, Don't Care Bits

Bit 3 **CLKINV** Output Clock Invert Bit

0 = Normal CLKOUT Polarity (as shown in the Timing Diagrams)

1 = Inverted CLKOUT Polarity

Bits 2-1 **CLKPHASE1: CLKPHASE0** Output Clock Phase Delay Bits

00 = No CLKOUT Delay (as shown in the Timing Diagrams)

01 = $CLKOUT^+/CLKOUT^-$ Delayed by 45° (Clock Period × 1/8)

10 = $CLKOUT^+/CLKOUT^-$ Delayed by 90° (Clock Period × 1/4)

11 = $CLKOUT^+/CLKOUT^-$ Delayed by 135° (Clock Period × 3/8)

Note: If the CLKOUT phase delay feature is used, the clock duty cycle stabilizer must also be turned on.

Bit 0 **DCS** Clock Duty Cycle Stabilizer Bit

0 = Clock Duty Cycle Stabilizer Off

1 = Clock Duty Cycle Stabilizer On

REGISTER A3: OUTPUT MODE REGISTER (ADDRESS 03h)

D7	D6	D5	D4	D3	D2	D1	D0
X	ILVDS2	ILVDS1	ILVDS0	TERMON	OUTOFF	OUTMODE1	OUTMODE0

Bit 7 Unused, Don't Care Bit

Bits 6-4 **ILVDS2: ILVDS0** LVDS Output Current Bits

000 = 3.5mA LVDS Output Driver Current

001 = 4.0mA LVDS Output Driver Current

010 = 4.5mA LVDS Output Driver Current

011 = Not Used

100 = 3.0mA LVDS Output Driver Current

101 = 2.5mA LVDS Output Driver Current

110 = 2.1mA LVDS Output Driver Current

111 = 1.75mA LVDS Output Driver Current

Bit 3 **TERMON** LVDS Internal Termination Bit

0 = Internal Termination Off

1 = Internal Termination On. LVDS output driver current is 2x the current set by ILVDS2:ILVDS0.

APPLICATIONS INFORMATION

Bit 2 **OUTOFF** Output Disable Bit

0 = Digital outputs are enabled.

1 = Digital outputs are disabled and have high output impedance.

Note: If the digital outputs are disabled the part should also be put in sleep mode or nap mode.

Bits 1-0 **OUTMODE1: OUTMODE0** Digital Output Mode Control Bits

00 = Full Rate CMOS Output Mode

01 = Double Data Rate LVDS Output Mode

10 = Double Data Rate CMOS Output Mode

11 = Not Used

REGISTER A4: DATA FORMAT REGISTER (ADDRESS 04h)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	OUTTEST2	OUTTEST1	OUTTEST0	ABP	RAND	TWOSCOMP

Bits 7-6 Unused, Don't Care Bits

Bits 5-3 **OUTTEST2: OUTTEST0** Digital Output Test Pattern Bits

000 = Digital Output Test Patterns Off

001 = All Digital Outputs = 0

011 = All Digital Outputs = 1

101 = Checkerboard Output Pattern. OF, D15-D0 alternate between 1 0101 0101 0101 0101 and 0 1010 1010 1010 1010.

111 = Alternating Output Pattern. OF, D15-D0 alternate between 0 0000 0000 0000 0000 and 1 1111 1111 1111 1111.

Note: Other bit combinations are not used.

Bit 2 **ABP** Alternate Bit Polarity Mode Control Bit

0 = Alternate Bit Polarity Mode Off

1 = Alternate Bit Polarity Mode On. Forces the output format to be Offset Binary.

Bit 1 **RAND** Data Output Randomizer Mode Control Bit

0 = Data Output Randomizer Mode Off

1 = Data Output Randomizer Mode On

Bits 0 **TWOSCOMP** Two's Complement Mode Control Bit

0 = Offset Binary Data Format

1 = Two's Complement Data Format

APPLICATIONS INFORMATION

GROUNDING AND BYPASSING

The LTC2162/LTC2161/LTC2160 requires a printed circuit board with a clean unbroken ground plane in the first layer beneath the ADC. A multilayer board with an internal ground plane is recommended. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

High quality ceramic bypass capacitors should be used at the V_{DD}, OV_{DD}, V_{CM}, V_{REF}, REFH and REFL pins. Bypass capacitors must be located as close to the pins as possible. Size 0402 ceramic capacitors are recommended. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

Of particular importance is the capacitor between REFH and REFL. This capacitor should be on the same side of the circuit board as the A/D, and as close to the device as possible.

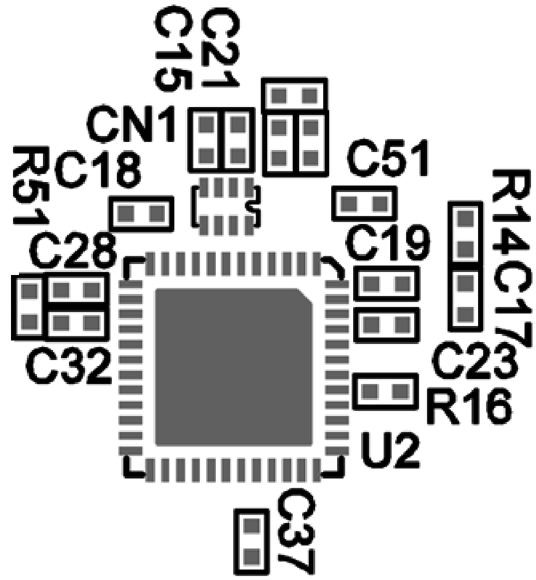
The analog inputs, encode signals, and digital outputs should not be routed next to each other. Ground fill and grounded vias should be used as barriers to isolate these signals from each other.

HEAT TRANSFER

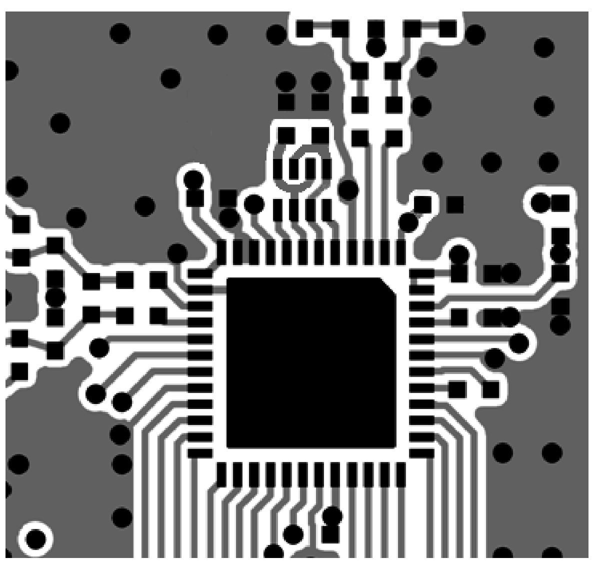
Most of the heat generated by the LTC2162/LTC2161/LTC2160 is transferred from the die through the bottom-side exposed pad and package leads onto the printed circuit board. For good electrical and thermal performance, the exposed pad must be soldered to a large grounded pad on the PC board. This pad should be connected to the internal ground planes by an array of vias.

TYPICAL APPLICATIONS

Silkscreen Top

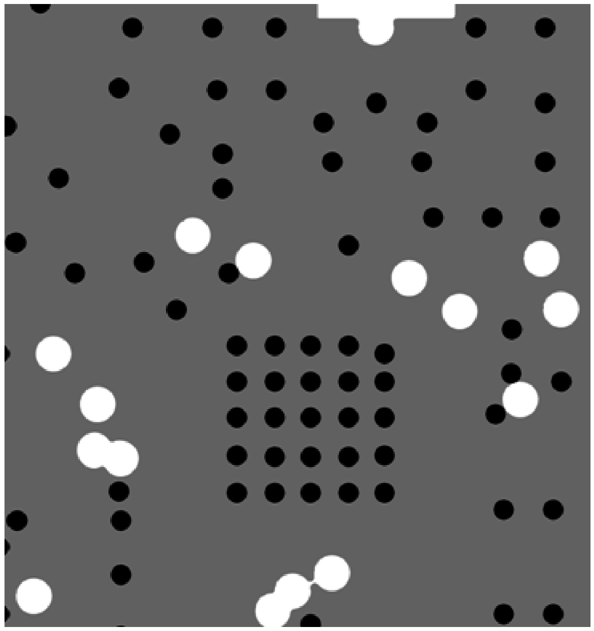


Top Side

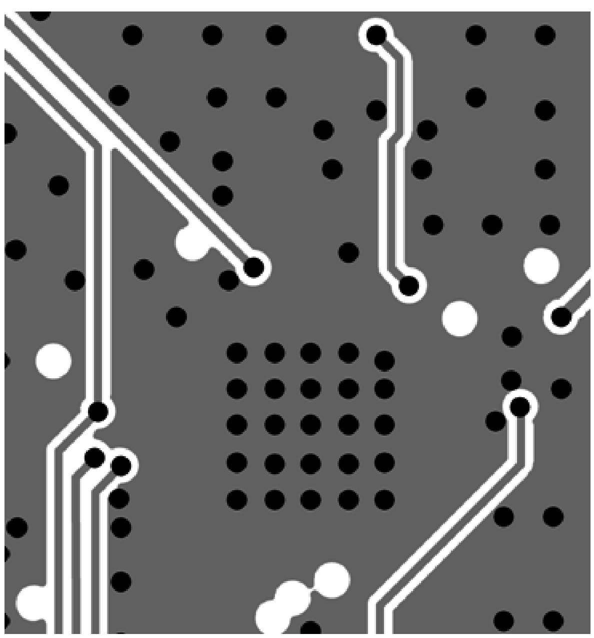


TYPICAL APPLICATIONS

Inner Layer 2

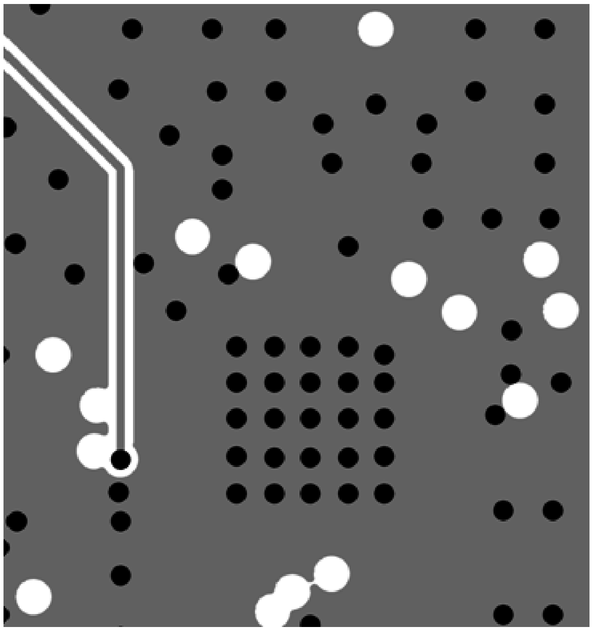


Inner Layer 3

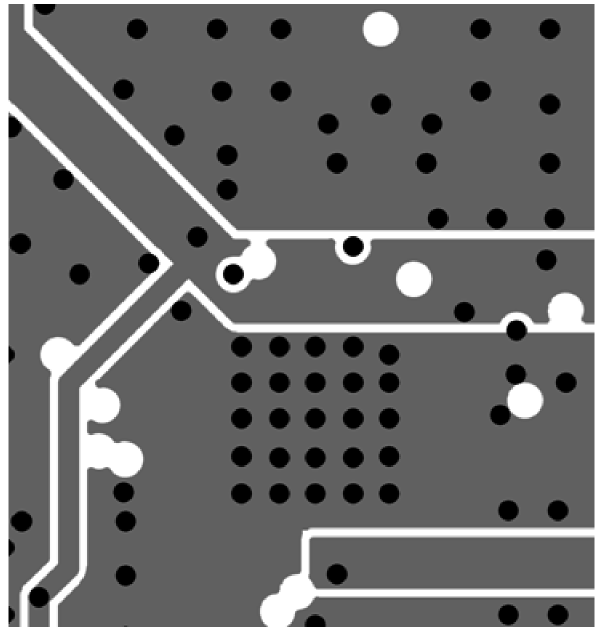


TYPICAL APPLICATIONS

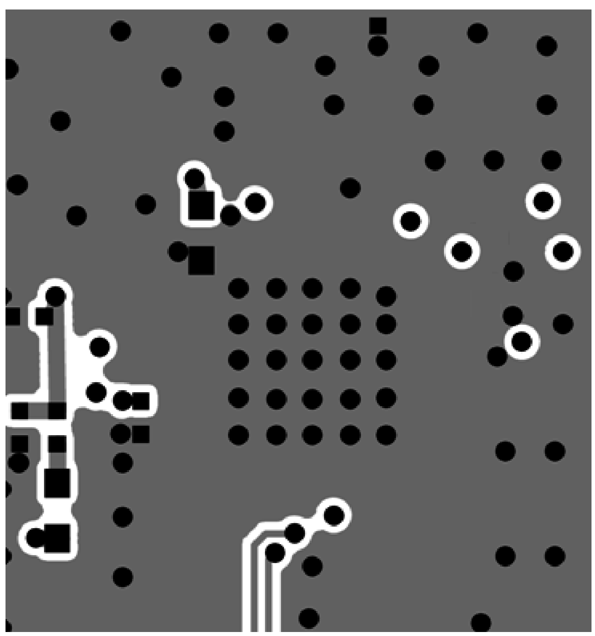
Inner Layer 4



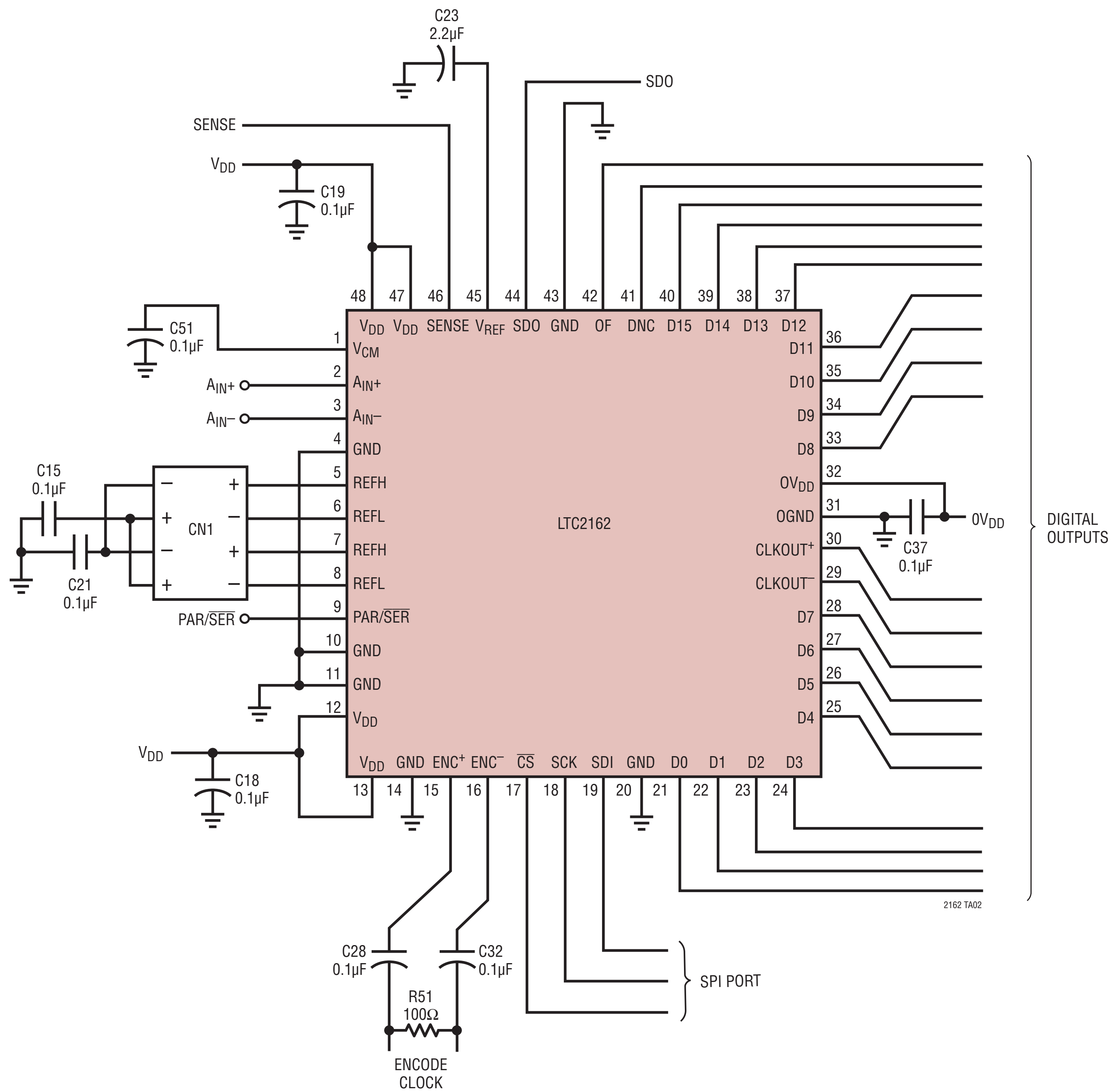
Inner Layer 5



Bottom Side

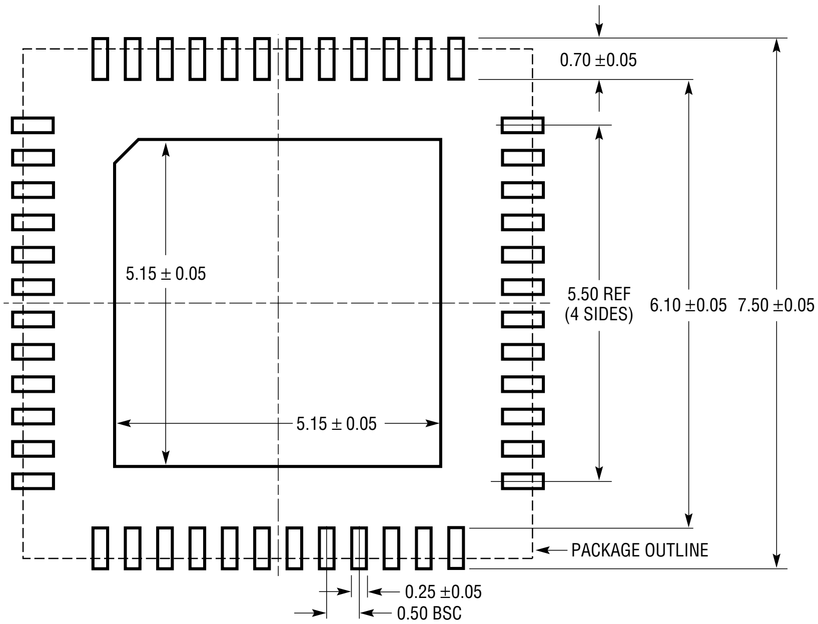


TYPICAL APPLICATIONS

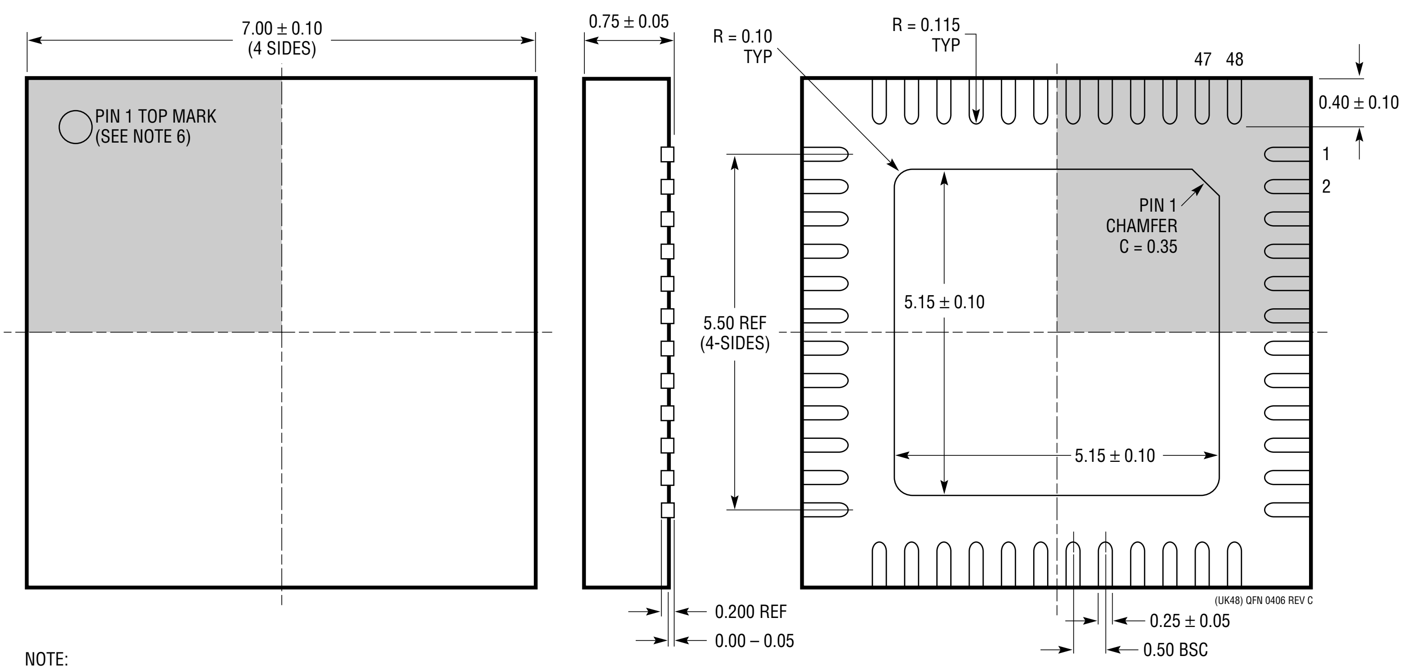


PACKAGE DESCRIPTION

UK Package
48-Lead Plastic QFN (7mm × 7mm)
(Reference LTC DWG # 05-08-1704 Rev C)



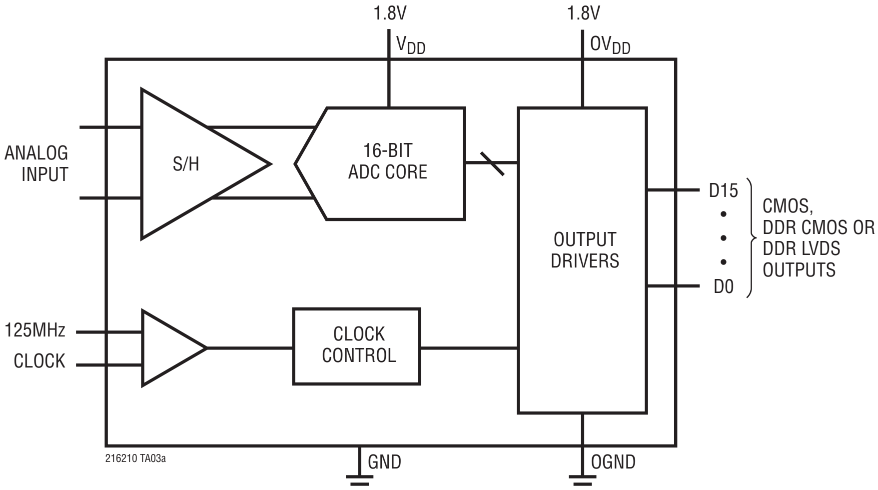
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



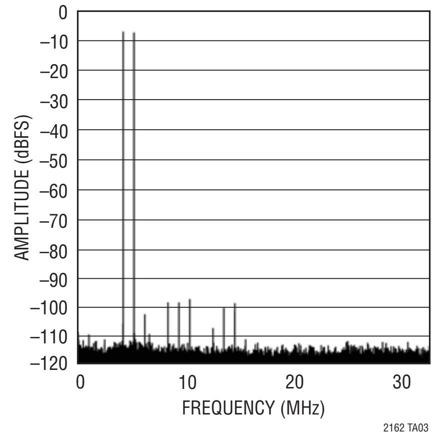
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WKKD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION



2-Tone FFT, f_{IN} = 70MHz and 69MHz



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC2259-14/LTC2260-14/ LTC2261-14	14-Bit, 80Msps/105Msps/125Msps 1.8V ADCs, Ultralow Power	89mW/106mW/127mW, 73.4dB SNR, 85dB SFDR, DDR LVDS/DDR CMOS/CMOS Outputs, 6mm × 6mm QFN-40
LTC2262-14	14-Bit, 150Msps 1.8V ADC, Ultralow Power	149mW, 72.8dB SNR, 88dB SFDR, DDR LVDS/DDR CMOS/CMOS Outputs, 6mm × 6mm QFN-40
LTC2266-14/LTC2267-14/ LTC2268-14	14-Bit, 80Msps/105Msps/125Msps 1.8V Dual ADCs, Ultralow Power	216mW/250mW/293mW, 73.4dB SNR, 85dB SFDR, Serial LVDS Outputs, 6mm × 6mm QFN-40
LTC2266-12/LTC2267-12/ LTC2268-12	12-Bit, 80Msps/105Msps/125Msps 1.8V Dual ADCs, Ultralow Power	216mW/250mW/293mW, 70.5dB SNR, 85dB SFDR, Serial LVDS Outputs, 6mm × 6mm QFN-40
LTC2208	16-Bit, 130Msps 3.3V ADC	1250mW, 77.7dB SNR, 100dB SFDR, CMOS/LVDS Outputs, 9mm × 9mm QFN-64
LTC2207/LTC2206	16-Bit, 105Msps/80Msps 3.3V ADCs	900mW/725mW, 77.9dB SNR, 100dB SFDR, CMOS Outputs, 7mm × 7mm QFN-48
LTC2217/LTC2216	16-Bit, 105Msps/80Msps 3.3V ADCs	1190mW/970mW, 81.2dB SNR, 100dB SFDR, CMOS/LVDS Outputs, 9mm × 9mm QFN-64
RF Mixers/Demodulators		
LTC5517	40MHz to 900MHz Direct Conversion Quadrature Demodulator	High IIP3: 21dBm at 800MHz, Integrated LO Quadrature Generator
LTC5527	400MHz to 3.7GHz High Linearity Downconverting Mixer	24.5dBm IIP3 at 900MHz, 23.5dBm IIP3 at 3.5GHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports
LTC5557	400MHz to 3.8GHz High Linearity Downconverting Mixer	23.7dBm IIP3 at 2.6GHz, 23.5dBm IIP3 at 3.5GHz, NF = 13.2dB, 3.3V Supply Operation, Integrated Transformer
LTC5575	800MHz to 2.7GHz Direct Conversion Quadrature Demodulator	High IIP3: 28dBm at 900MHz, Integrated LO Quadrature Generator, Integrated RF and LO Transformer
Amplifiers/Filters		
LTC6412	800MHz, 31dB Range, Analog-Controlled Variable Gain Amplifier	Continuously Adjustable Gain Control, 35dBm OIP3 at 240MHz, 10dB Noise Figure, 4mm × 4mm QFN-24
LTC6420-20	1.8GHz Dual Low Noise, Low Distortion Differential ADC Drivers for 300MHz IF	Fixed Gain 10V/V, $1nV/\sqrt{Hz}$ Total Input Noise, 80mA Supply Current per Amplifier, 3mm × 4mm QFN-20
LTC6421-20	1.3GHz Dual Low Noise, Low Distortion Differential ADC Drivers	Fixed Gain 10V/V, $1nV/\sqrt{Hz}$ Total Input Noise, 40mA Supply Current per Amplifier, 3mm × 4mm QFN-20
LTC6605-7/LTC6605-10/ LTC6605-14	Dual Matched 7MHz/10MHz/14MHz Filters with ADC Drivers	Dual Matched 2nd Order Lowpass Filters with Differential Drivers, Pin-Programmable Gain, 6mm × 3mm DFN-22
Signal Chain Receivers		
LTM9002	14-Bit Dual Channel IF/Baseband Receiver Subsystem	Integrated High Speed ADC, Passive Filters and Fixed Gain Differential Amplifiers

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0711 • PRINTED IN USA