

## FEATURES

- Software-Selectable Cable Termination for:
  - RS232 (V.28)
  - RS423 (V.10)
  - RS422 (V.11)
  - RS485
  - RS449
  - EIA530
  - EIA530-A
  - V.35
  - V.36
  - X.21
- Outputs Won't Load the Line with Power Off


## APPLICATIONS

- Data Networking
- CSU and DSU
- Data Routers

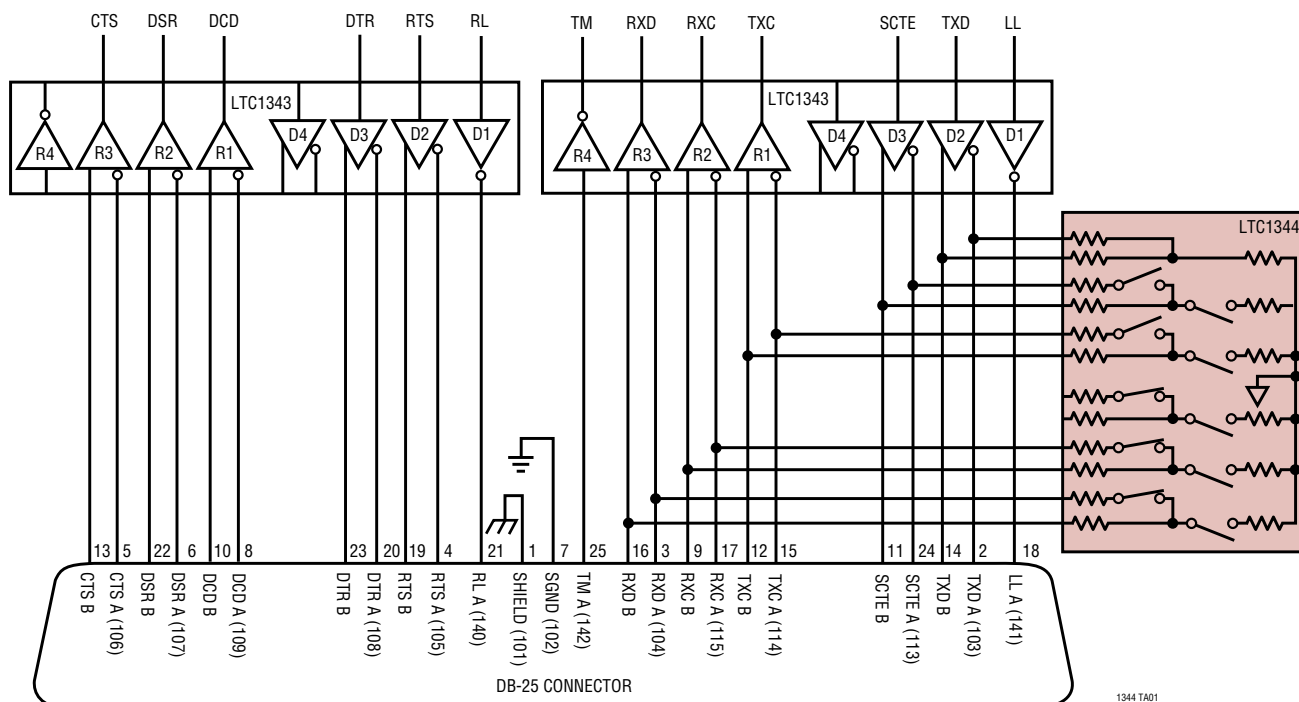
## DESCRIPTION

The LTC<sup>®</sup>1344 features six software-selectable multiprotocol cable terminators. Each terminator can be configured as an RS422 (V.11) 100Ω minimum differential load, V.35 T-network load or an open circuit for use with RS232 (V.28) or RS423 (V.10) transceivers that provide their own termination. When combined with the LTC1343, the LTC1344 forms a complete software-selectable multiprotocol serial port. A data bus latch feature allows sharing of the select lines between multiple interface ports.

The LTC1344 is available in a 24-lead SSOP.

 LTC and LT are registered trademarks of Linear Technology Corporation.

## TYPICAL APPLICATION



## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Positive Supply Voltage ( $V_{CC}$ )	7V
Negative Supply Voltage ( $V_{EE}$ )	-13.2V
Input Voltage (Logic Inputs) .... $V_{EE} - 0.3V$ to $V_{CC} + 0.3V$	
Input Voltage (Load Inputs)	$\pm 18V$
Operating Temperature Range	
LTC1344C	0°C to 70°C
LTC1344I	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

## PACKAGE/ORDER INFORMATION

TOP VIEW		ORDER PART NUMBER
M0	1	24 M1
$V_{EE}$	2	23 M2
R1C	3	22 DCE/DTE
R1B	4	21 LATCH
R1A	5	20 R6B
R2A	6	19 R6A
R2B	7	18 R5A
R2C	8	17 R5B
R3A	9	16 R4A
R3B	10	15 R4B
R3C	11	14 $V_{CC}$
GND	12	13 GND
G PACKAGE 24-LEAD PLASTIC SSOP $T_{JMAX} = 150^{\circ}C$ , $\theta_{JA} = 100^{\circ}C/W$		LTC1344CG LTC1344IG

Consult factory for Military grade parts.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}C$ .  
 $V_{CC} = 5V \pm 5\%$ ,  $V_{EE} = -5V \pm 5\%$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$  (Notes 2, 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Supplies</b>						
$I_{CC}$	Supply Current	All Digital Pins = GND or $V_{CC}$	●	200	700	$\mu A$
<b>Terminator Pins</b>						
$R_{V,35}$	Differential Mode Impedance Common Mode Impedance	All Loads (Figure 1), $-2V \leq V_{CM} \leq 2V$ (Commercial)	●	90	103	110 $\Omega$
		All Loads (Figure 2), $-2V \leq V_{CM} \leq 2V$ (Commercial)	●	135	153	165 $\Omega$
		All Loads (Figure 1), $-2V \leq V_{CM} \leq 2V$ (Industrial)	●	90	104	125 $\Omega$
		All Loads (Figure 2), $-2V \leq V_{CM} \leq 2V$ (Industrial)	●	130	153	170 $\Omega$
$R_{V,11}$	Differential Mode Impedance	All Loads (Figure 1), $-7V \leq V_{CM} \leq 7V$ (Commercial)		100	104	$\Omega$
		All Loads (Figure 1), $V_{CM} = 0V$ (Commercial)	●	100	104	110 $\Omega$
		All Loads (Figure 1), $V_{CM} = 0V$ (Industrial)	●	95	104	125 $\Omega$
$I_{LEAK}$	High Impedance Leakage Current	All Loads, $-7V \leq V_{CM} \leq 7V$ (Commercial)	●	$\pm 1$	$\pm 50$	$\mu A$
<b>Logic Inputs</b>						
$V_{IH}$	Input High Voltage	All Logic Input Pins	●	2		V
$V_{IL}$	Input Low Voltage	All Logic Input Pins	●		0.8	V
$I_{IN}$	Input Current	All Logic Input Pins	●		$\pm 10$	$\mu A$

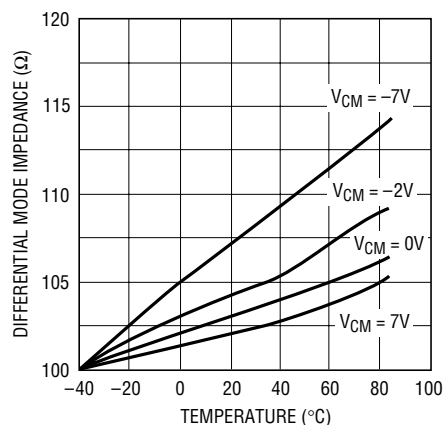
**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are reference to ground unless otherwise specified.

**Note 3:** All typicals are given at  $V_{CC} = 5V$ ,  $V_{EE} = -5V$ ,  $T_A = 25^{\circ}C$ .

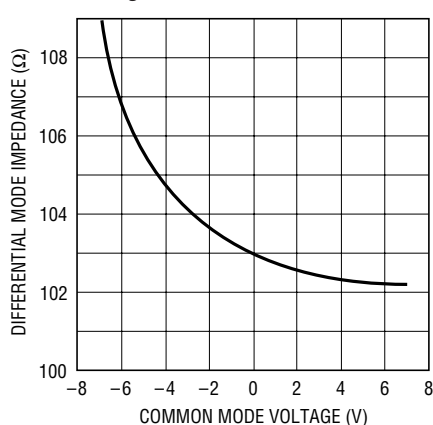
# TYPICAL PERFORMANCE CHARACTERISTICS

**V.11 or V.35 Differential Mode Impedance vs Temperature**



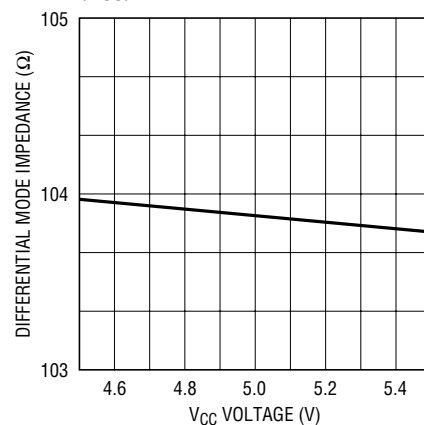
1344 G01

**V.11 or V.35 Differential Mode Impedance vs Common Mode Voltage**



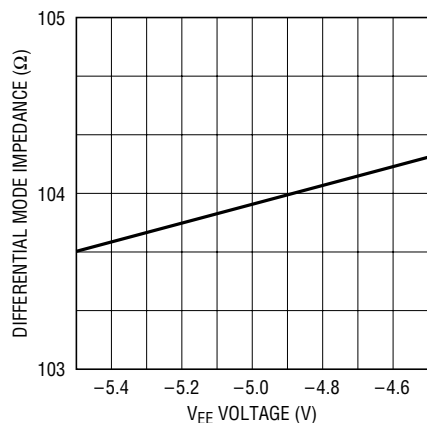
1344 G02

**V.11 or V.35 Differential Mode Impedance vs Supply Voltage ( $V_{CC}$ )**



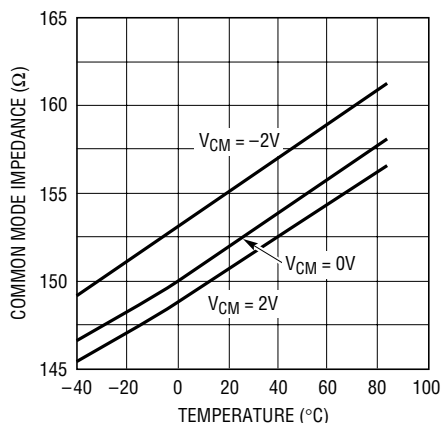
1344 G03

**V.11 or V.35 Differential Mode Impedance vs Negative Supply Voltage ( $V_{EE}$ )**



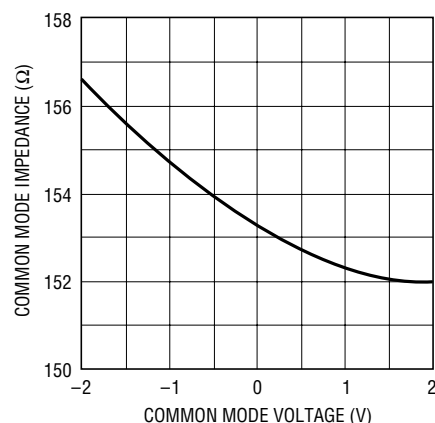
1344 G04

**V.35 Common Mode Impedance vs Temperature**



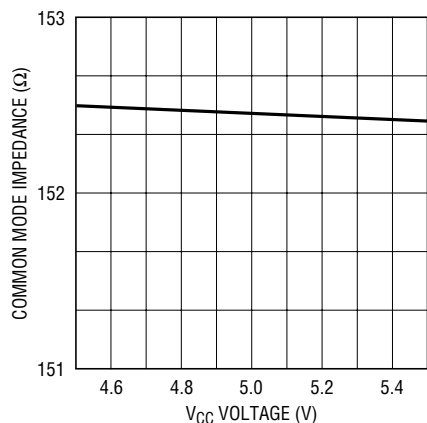
1344 G05

**V.35 Common Mode Impedance vs Common Mode Voltage**



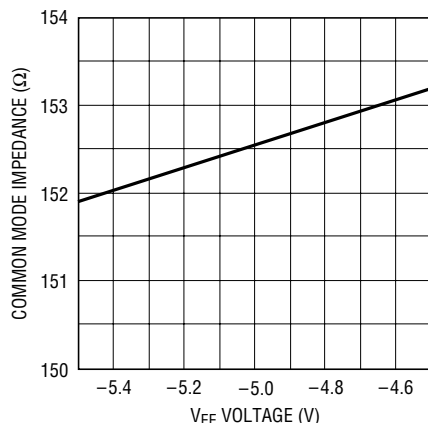
1344 G06

**V.35 Common Mode Impedance vs Supply Voltage ( $V_{CC}$ )**



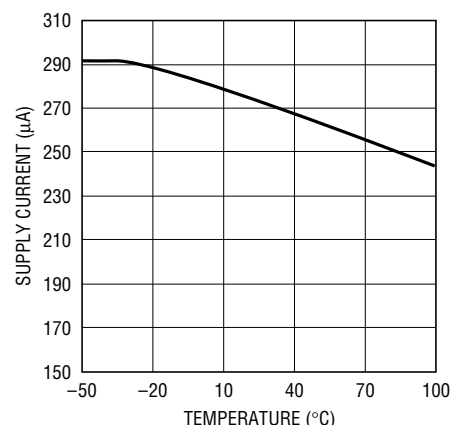
1344 G07

**V.35 Common Mode Impedance vs Negative Supply Voltage ( $V_{EE}$ )**



1344 G08

**Supply Current vs Temperature**



1344 G09

## PIN FUNCTIONS

**M0 (Pin 1):** TTL Level Mode Select Input. The data on M0 is latched when  $\overline{\text{LATCH}}$  is high.

**V<sub>EE</sub> (Pin 2):** Negative Supply Voltage Input. Can connect directly to the LTC1343 V<sub>EE</sub> pin.

**R1C (Pin 3):** Load 1 Center Tap.

**R1B (Pin 4):** Load 1 Node B.

**R1A (Pin 5):** Load 1 Node A.

**R2A (Pin 6):** Load 2 Node A.

**R2B (Pin 7):** Load 2 Node B.

**R2C (Pin 8):** Load 2 Center Tap.

**R3A (Pin 9):** Load 3 Node A.

**R2B (Pin 10):** Load 2 Node B.

**R3C (Pin 11):** Load 3 Center Tap.

**GND (Pin 12):** Ground Connection for Load 1 to Load 3.

**GND (Pin 13):** Ground Connection for Load 4 to Load 6.

**V<sub>CC</sub> (Pin 14):** Positive Supply Input.  $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$ .

**R4B (Pin 15):** Load 4 Node B.

**R4A (Pin 16):** Load 4 Node A.

**R5B (Pin 17):** Load 5 Node B.

**R5A (Pin 18):** Load 5 Node A.

**R6A (Pin 19):** Load 6 Node A.

**R6B (Pin 20):** Load 6 Node B.

**$\overline{\text{LATCH}}$  (Pin 21):** TTL Level Logic Signal Latch Input. When it is low the input buffers on M0, M1, M2 and DCE/DTE are transparent. When it is high the logic pins are latched into their respective input buffers. The data latch allows the select lines to be shared between multiple I/O ports.

**DCE/ $\overline{\text{DTE}}$  (Pin 22):** TTL Level Mode Select Input. The DCE mode is selected when it is high and DTE mode when low. The data on DCE/ $\overline{\text{DTE}}$  is latched when  $\overline{\text{LATCH}}$  is high.

**M2 (Pin 23):** TTL Level Mode Select Input 1. The data on M2 is latched when  $\overline{\text{LATCH}}$  is high.

**M1 (Pin 24):** TTL Level Mode Select Input 2. The data on M1 is latched when  $\overline{\text{LATCH}}$  is high.

## TEST CIRCUITS

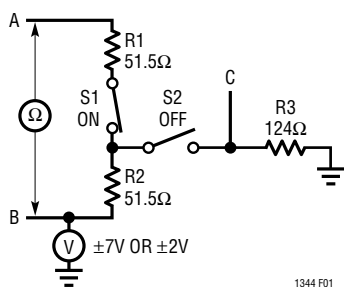


Figure 1. Differential V.11 or V.35 Impedance Measurement

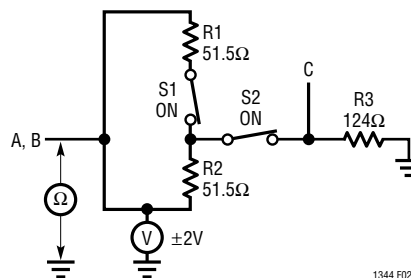


Figure 2. V.35 Common Mode Impedance Measurement

## MODE SELECTION

LTC1344 MODE NAME	DCE/DTE	M2	M1	M0	R1	R2	R3	R4	R5	R6
V.10/RS423	X	0	0	0	Z	Z	Z	Z	Z	Z
RS530A	0	0	0	1	Z	Z	Z	V.11	V.11	V.11
	1	0	0	1	Z	Z	Z	Z	V.11	V.11
Reserved	0	0	1	0	Z	Z	Z	V.11	V.11	V.11
	1	0	1	0	V.11	V.11	V.11	Z	Z	Z
X.21	0	0	1	1	Z	Z	Z	V.11	V.11	V.11
	1	0	1	1	Z	Z	Z	Z	V.11	V.11
V.35	0	1	0	0	V.35	V.35	Z	V.35	V.35	V.35
	1	1	0	0	V.35	V.35	V.35	Z	V.35	V.35
RS530/RS449/V.36	0	1	0	1	Z	Z	Z	V.11	V.11	V.11
	1	1	0	1	Z	Z	Z	Z	V.11	V.11
V.28/RS232	X	1	1	0	Z	Z	Z	Z	Z	Z
No Cable	X	1	1	1	V.11	V.11	V.11	V.11	V.11	V.11

X = don't care, 0 = logic low, 1 = logic high

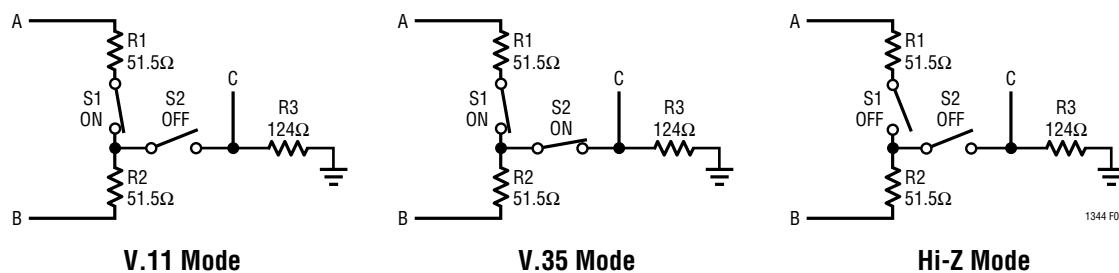


Figure 3. LTC1344 Modes

## APPLICATIONS INFORMATION

### Multiprotocol Cable Termination

One of the most difficult problems facing the designer of a multiprotocol serial interface is how to allow the transmitters and receivers for different electrical standards to share connector pins. In some cases the transmitters and receivers for each interface standard can be simply tied together and the appropriate circuitry enabled. But the biggest problem still remains: how to switch the various cable terminations required by the different standards.

Traditional implementations have included switching resistors with expensive relays or requiring the user to change termination modules every time the interface standard has changed. Custom cables have been used with the termination in the cable head or separate terminations are built on the board, and a custom cable routes the signals to the appropriate termination. Switching the terminations using FETs is difficult because the FETs must remain off even though the signal voltage is beyond the supply voltage for the FET drivers or the power is off.

The LTC1344 solves the cable termination switching problem via software control. The LTC1344 provides termination for the V.10 (RS423), V.11 (RS422), V.28 (RS232) and V.35 electrical protocols.

### V.10 (RS423) Termination

A typical V.10 unbalanced interface is shown in Figure 4. A V.10 single-ended generator output A with ground C is connected to a differential receiver with inputs A' connected to A and input B' connected to the signal return ground C. The receiver's ground C' is separate from the signal return. Usually no cable termination is required for V.10 interfaces but the receiver inputs must be compliant with the impedance curve shown in Figure 5.

In V.10 mode, both switches S1 and S2 are turned off so the only cable termination is the input impedance of the V.10 receiver.

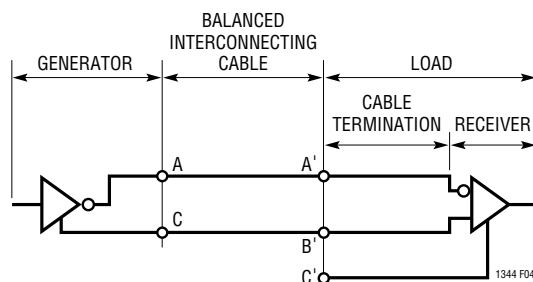


Figure 4. Typical V.10 Interface

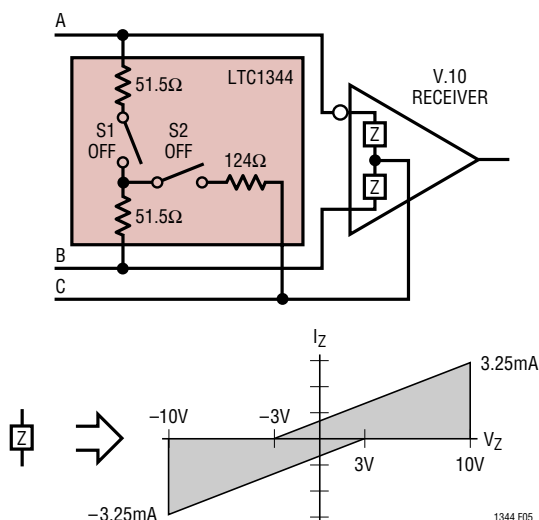


Figure 5. V.10 Interface Using the LTC1344

### V.11 (RS422) Termination

A typical V.11 balanced interface is shown in Figure 6. A V.11 differential generator with outputs A and B with ground C is connected to a differential receiver with ground C', inputs A' connected to A, B' connected to B. The V.11 interface requires a different termination at the receiver end that has a minimum value of 100Ω. The receiver inputs must also be compliant with the impedance curve shown in Figure 7.

In V.11 mode, switch S1 is turned on and S2 is turned off so the cable is terminated with a 103Ω impedance.

## APPLICATIONS INFORMATION

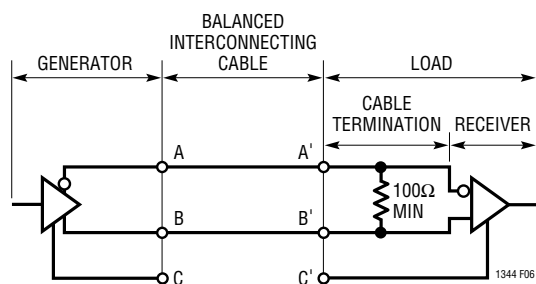


Figure 6. Typical V.11 Interface

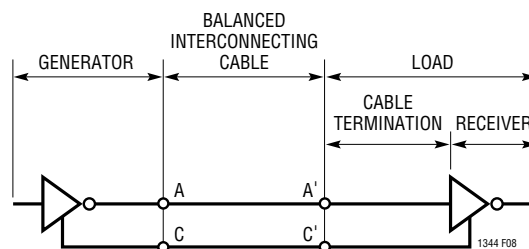


Figure 8. Typical V.28 Interface

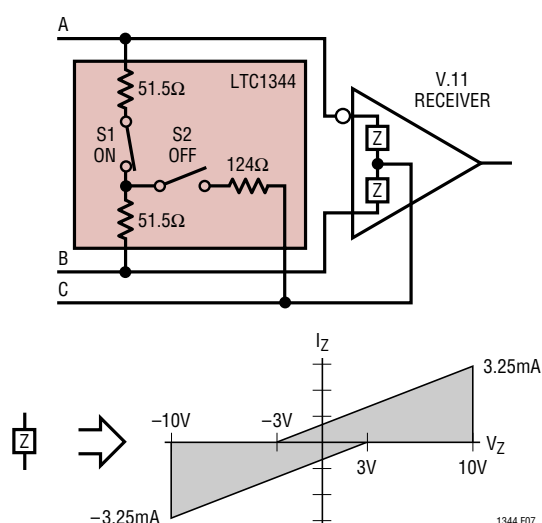


Figure 7. V.11 Interface Using the LTC1344

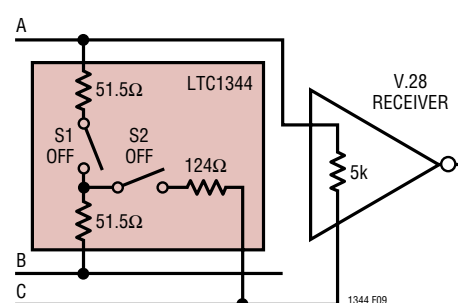


Figure 9. V.28 Interface Using the LTC1344

### V.28 (RS232) Termination

A typical V.28 unbalanced interface is shown in Figure 8. A V.28 single-ended generator output A with ground C is connected to a single-ended receiver with inputs A' connected to A, ground C' connected via the signal return ground to C. The V.28 standard requires a 5k terminating resistor to ground which is included in almost all compliant receivers as shown in Figure 9. Because the termination is included in the receiver, both switches S1 and S2 in the LTC1344 are turned off.

### V.35 Termination

A typical V.35 balanced interface is shown in Figure 10. A V.35 differential generator with outputs A and B with ground C is connected to a differential receiver with ground C', inputs A' connected to A, B' connected to B. The V.35 interface requires a T-network termination at the receiver end and the generator end. In V.35 mode both switches S1 and S2 in the LTC1344 are turned on as shown in Figure 11.

The differential impedance measured at the connector must be  $100\Omega \pm 10\Omega$  and the impedance between shorted terminals A' and B' to ground C' must be  $150\Omega \pm 15\Omega$ . The input impedance of the V.35 receiver is connected in parallel with the T-network inside the LTC1344, which can cause the overall impedance to fail the specification on the

## APPLICATIONS INFORMATION

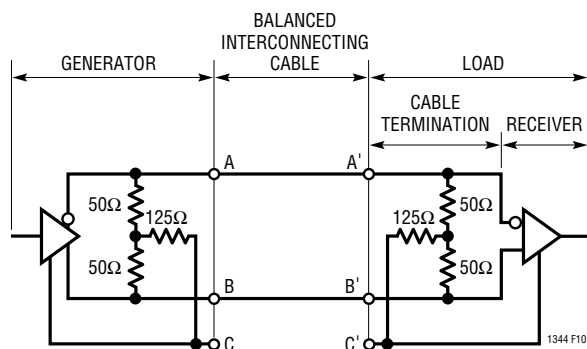


Figure 10. Typical V.35 Interface

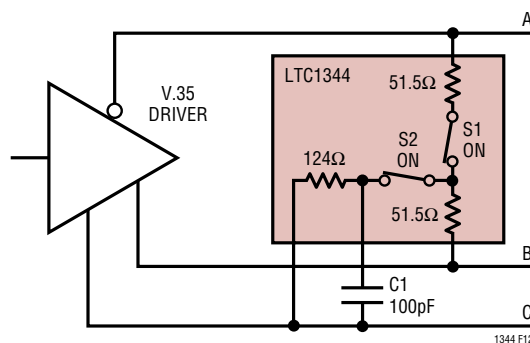


Figure 12. V.35 Driver Using the LTC1344

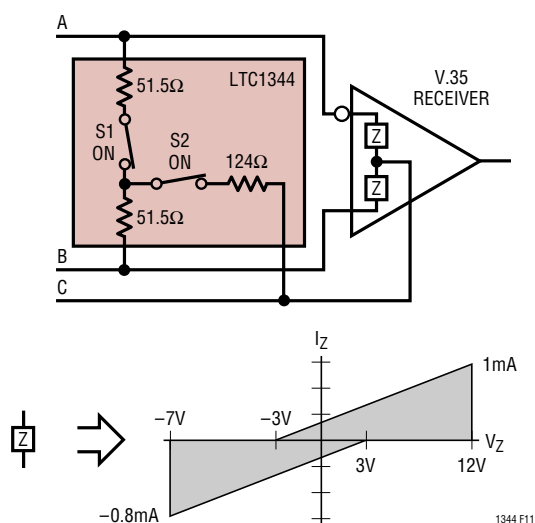


Figure 11. V.35 Receiver Using the LTC1344

low side. However, all of Linear Technology's V.35 receivers meet the RS485 input impedance specification as shown in Figure 11, which insures compliance with the V.35 specification when used with the LTC1344.

The generator differential impedance must be  $50\Omega$  to  $150\Omega$  and the impedance between shorted terminals A

and B to ground C must be  $150\Omega \pm 15\Omega$ . For the generator termination, switches S1 and S2 are both on and the top side of the center resistor is brought out to a pin so it can be bypassed with an external capacitor to reduce common mode noise as shown in Figure 12.

Any mismatch in the driver rise and fall times or skew in the driver propagation delays will force current through the center termination resistor to ground causing a high frequency common mode spike on the A and B terminals. The common mode spike can cause EMI problems that are reduced by capacitor C1 which shunts much of the common mode energy to ground rather than down the cable.

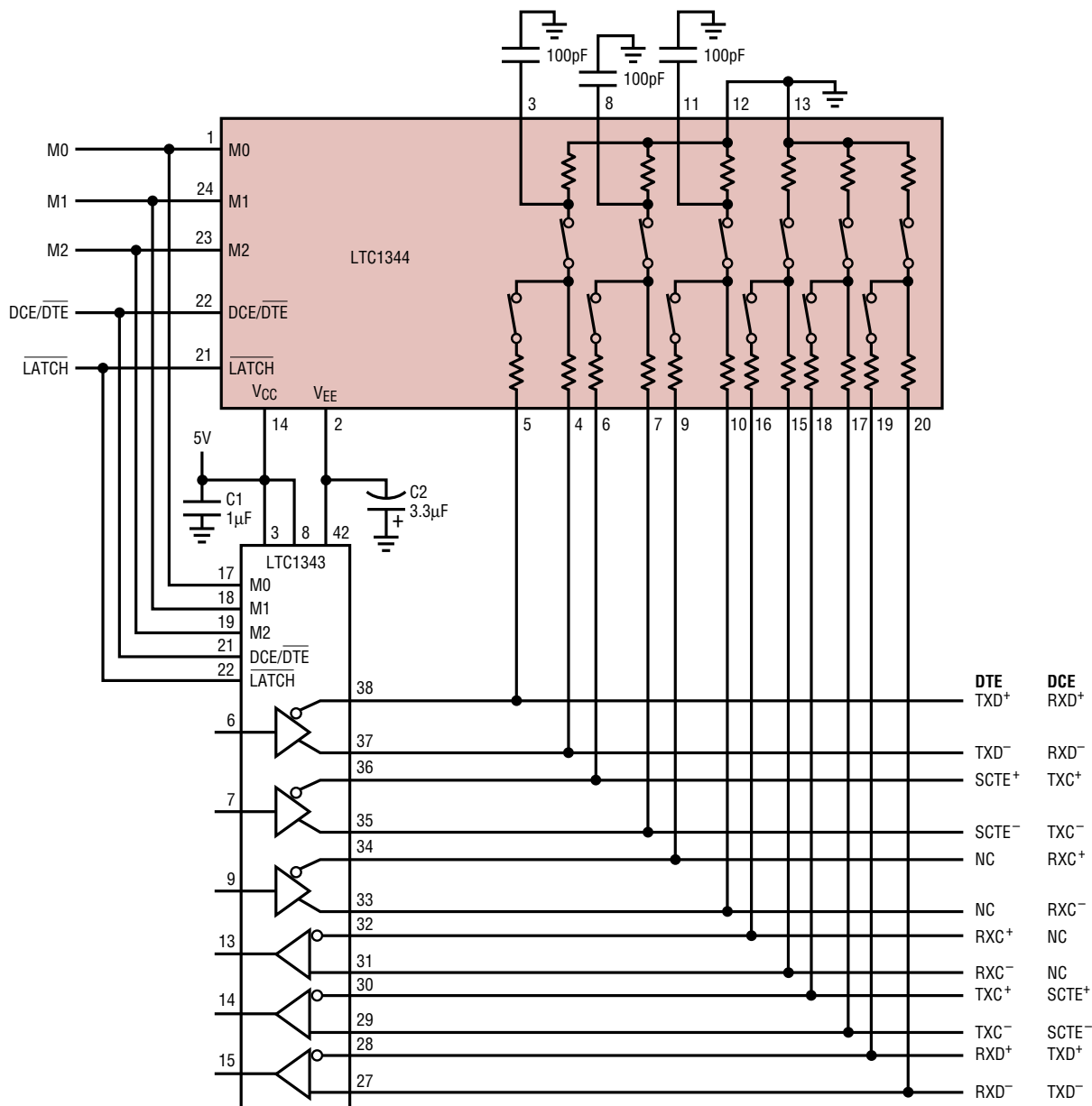
### The LATCH Pin

The LATCH pin (21) allows the select lines (M0, M1, M2 and DCE/DTE) to be shared with multiple LTC1344s, each with its own LATCH signal. When the LATCH pin is held low the select line input buffers are transparent. When the LATCH pin is pulled high, the select line input buffers latch the state of the Select pins so that changes on the select lines are ignored until LATCH is pulled low again. If the latch feature is not used, the LATCH pin should be tied to ground.

## TYPICAL APPLICATIONS

Figure 13 shows a typical application for the LTC1344 using the LTC1343 mixed mode transceiver chip to generate the clock and data signals for a serial interface. The LTC1344  $V_{EE}$  supply is generated from the LTC1343 charge pump and the select lines M0, M1, M2, DCE and

LATCH are shared by both chips. Each driver output and receiver input is connected to one of the LTC1344 termination ports. Each electrical protocol can then be chosen using the digital select lines.



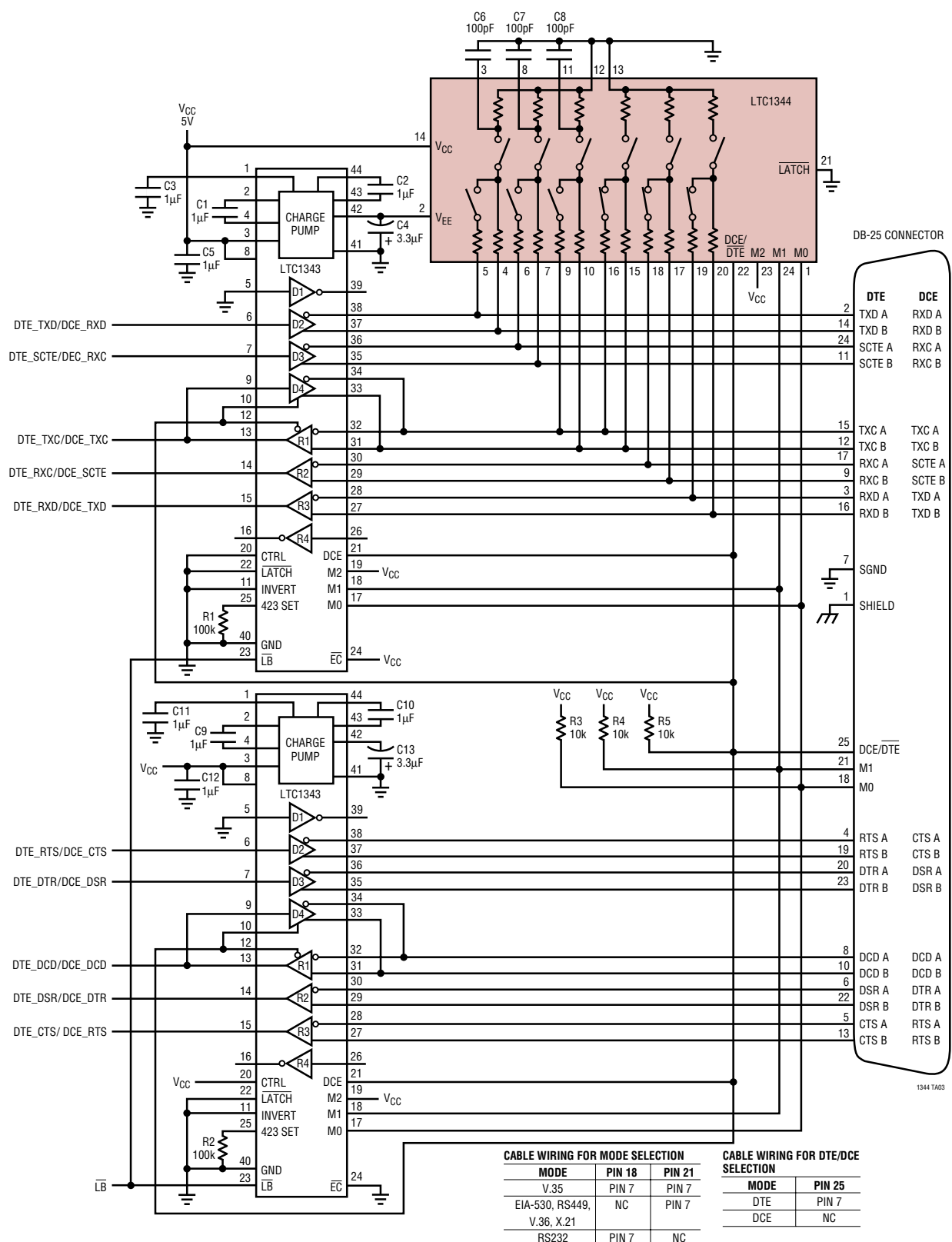
1344 F13

Figure 13. Typical Application Using the LTC1344

The schematic diagram illustrates the internal components and connections of the LTC1344 evaluation board. It features two LTC1344 chips, each containing a charge pump, four comparators (D1-D4), and a 4x4 switch matrix. The top chip's charge pump is powered by a 5V VCC pin, with capacitors C1, C2, C3, C4, C5, C6, C7, and C8. The bottom chip's charge pump is powered by a VCC pin, with capacitors C9, C10, C11, C12, and C13. Both chips have a 3.3μF capacitor (C4 and C13) connected to their VEE pins. The comparators are configured with various feedback resistors (R1, R2, R3, R4) and a 100kΩ resistor (R1 and R2). The 4x4 switch matrix is controlled by DTE/DCE signals (LL, TXD, RXD, SCTE, RXC, TM) and outputs to a DB-25 connector. The connector pins are labeled with DTE and DCE signals, including LL A, TXD A, RXD A, SCTE A, RXC A, TM A, TXC A, TXC B, SCTE B, SCTE B, RXD A, RXD B, TXD B, LL A, RL A, RTS A, CTS A, DTR A, DSR A, DCD A, DCD B, DSR A, DTR A, DSR B, DTR B, CTS A, RTS A, CTS B, and RTS B. The diagram also shows the internal components of the LTC1344, including the charge pump, comparators, and the 4x4 switch matrix.

## TYPICAL APPLICATIONS

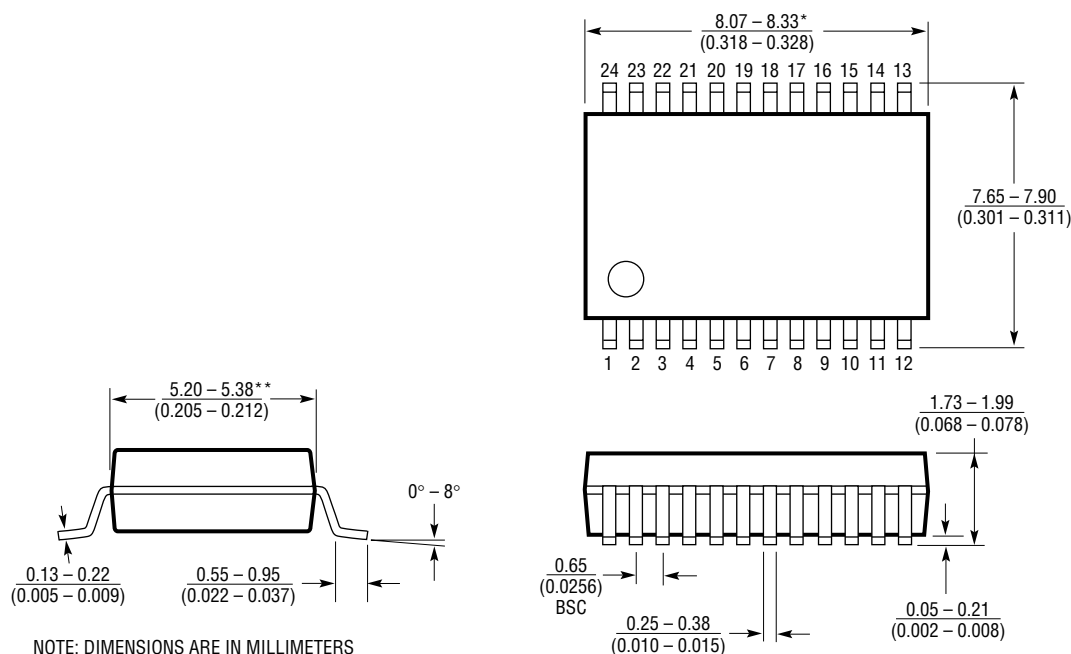
Cable Selectable Multiprotocol DTE Port with DB-25 Connector



**PACKAGE DESCRIPTION**

Dimensions in inches (millimeters) unless otherwise noted.

**G Package**  
**24-Lead Plastic SSOP (0.209)**  
 (LTC DWG # 05-08-1640)



G24 SSOP 1098

**RELATED PARTS**

PART NUMBER	DESCRIPTION	COMMENTS
LTC1334	Single Supply RS232/RS485 Transceiver	2 RS485 Dr/Rx or 4 RS232 Dr/Rx Pairs
LTC1343	Multiprotocol Serial Transceiver	Software Selectable Multiprotocol Interface
LTC1345	Single Supply V.35 Transceiver	3 Dr/3 Rx for Data and CLK Signals
LTC1346A	Dual Supply V.35 Transceiver	3 Dr/3 Rx for Data and CLK Signals
LTC1344A	Multiprotocol Cable Terminator, Pin Compatible to LTC1344	Allows Separate RS449 Mode
LTC1543	Multiprotocol Serial Transceiver	3 Dr/3 Rx for Data and CLK Signals
LTC1544	Multiprotocol Serial Transceiver	4 Dr/4 Rx for Control Signals and LL
LTC1545	Multiprotocol Serial Transceiver	5 Dr/5 Rx for Control Signals, LL, RL and TM