High Performance, 12-Bit, 12-Channel Decimating, LCD DecDriver®

AD8387

FEATURES

High accuracy, high-resolution voltage outputs
- **1 mV channel matching**
- **12-bit input resolution**
- **Laser-trimmed outputs**

Fast settling, high voltage drive
- **35 ns settling time to 0.25% into 150 pF load**
- **Slew rate 420 V/µs**
- **Outputs to within 1.3 V of supply rails**

High update rates
- **Fast, 110 MHz clock**

Programmable video reference (brightness) and full-scale (contrast) output levels

Flexible logic
- **INV bit reverses polarity of video signal**
- **R/L reverses loading order of data**
- **ISW selects frame/row or column/dot inversion**
- **DSW selects single or dual data bus mode**

Output short-circuit protection

3.3 V logic, 11 V to 18 V analog supplies

Available in 80-lead, 12 mm × 12 mm, TQFP E-pad

APPLICATIONS

LCD microdisplay driver

FUNCTIONAL BLOCK DIAGRAM

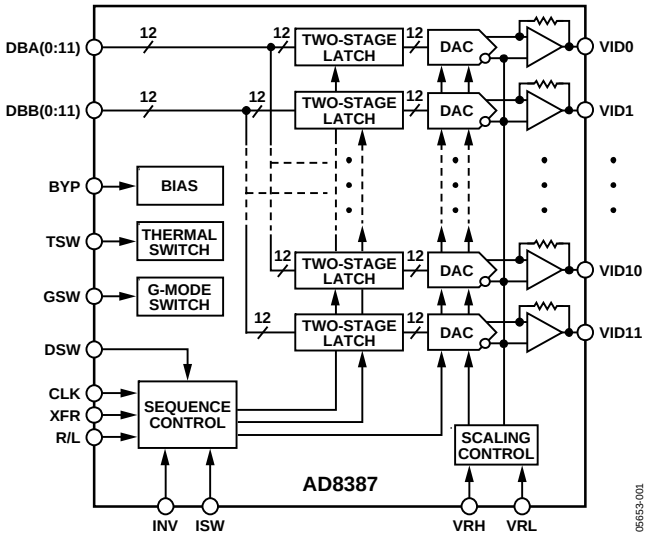

Figure 1.

GENERAL DESCRIPTION

The AD8387 DecDriver provides dual, fast latched, 12-bit decimating input, which drives 12 high voltage outputs. Twelve-bit input words are loaded into 12 separate high speed, bipolar DACs sequentially. Flexible digital input format allows more than one AD8387 to be used in parallel for higher resolution displays. The output signal can be adjusted for dc reference, signal inversion, and contrast for maximum flexibility.

The AD8387 is fabricated on ADI's fast bipolar, 26 V XFCB process, providing fast input logic, bipolar DACs with trimmed accuracy and fast settling, high voltage, precision drive amplifiers on the same chip.

The AD8387 dissipates 1.34 W nominal static power. The AD8387 is offered in an 80-lead TQFP E-pad package and operates over the commercial temperature range of 0°C to +85°C.

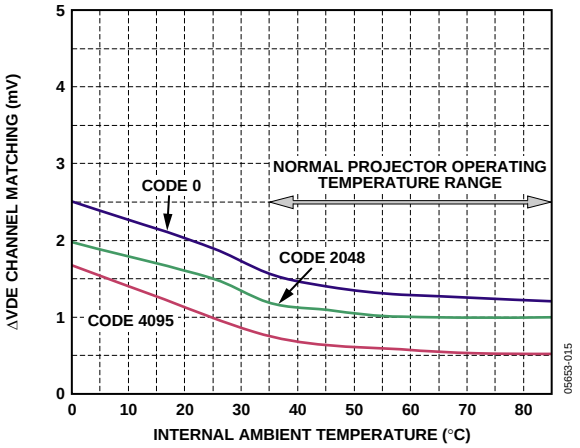

Figure 2. Channel Matching vs. Temperature

Rev. 0

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REVISION HISTORY

10/05—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, AVCC = 15.5 V, DVCC = 3.3 V, VRH = 9.5 V, VRL = 7 V, $T_{A\,MIN}$ = 0°C, $T_{A\,MAX}$ = 75°C still air, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
VIDEO DC PERFORMANCE[1]	$T_{A\,MIN}$ to $T_{A\,MAX}$, VFS = 5 V				
VDE—Differential Error Voltage	@ DAC code 0	−5.5	−0.8	+5.0	mV
	@ DAC code 1024	−4.4	−0.5	+3.6	mV
	@ DAC code 2048	−3.6	−0.3	+3.3	mV
	@ DAC code 3072	−2.8	−0.3	+2.8	mV
	@ DAC code 4095	−2.1	+0.2	+2.1	mV
	DAC code range 0 to 4095	−6.0		+6.0	mV
VCME—Common-Mode Error Voltage	@ DAC code 0	−2.5	−0.3	+2.5	mV
	@ DAC code 1024	−2.5	−0.3	+2.5	mV
	@ DAC code 2048	−2.5	−0.3	+2.5	mV
	@ DAC code 3072	−2.5	−0.3	+2.5	mV
	@ DAC code 4095	−2.5	−0.3	+2.5	mV
	DAC code range 0 to 4095	−3.5		+3.5	mV
ΔVDE—VDE Channel Matching	@ DAC code 0		1.9	4.8	mV
	@ DAC code 1024		1.8	4.3	mV
	@ DAC code 2048		1.6	4.0	mV
	@ DAC code 3072		1.4	3.8	mV
	@ DAC code 4095		1.0	2.8	mV
	DAC code range 0 to 4095			5.5	mV
ΔV—Channel Matching	@ DAC code 0		2.7		mV
	@ DAC code 1024		2.7		mV
	@ DAC code 2048		2.5		mV
	@ DAC code 3072		2.5		mV
	@ DAC code 4095		2.0		mV
	DAC code range 0 to 4095			7.5	mV
DNL[2]		−1	−0.2		LSB
VIDEO OUTPUT DYNAMIC PERFORMANCE	$T_{A\,MIN}$ to $T_{A\,MAX}$				
Data Switching Settling Time to 0.25%	VIDx = 5 V step, C_L = 150 pF		35	50	ns
Data Switching Settling Time to 1%			22	28	ns
Data Switching Slew Rate	20% to 80%		420		V/µs
CLK and Data Feedthrough[3]			15		mV p-p
All-Hostile Crosstalk[4]					
Amplitude			69		mV p-p
Glitch Duration			50		ns
DAC Transition Glitch Energy	DAC Code 2047 to 2048		0.4		nV-s
Invert Switching Settling Time to 0.25%	VIDx = 10 V step, C_L = 150 pF		70	150	ns
Invert Switching Settling Time to 1%			34	40	ns
Invert Switching Slew Rate	20% to 80%		700		V/µs
Invert Switching Overshoot			25		mV

Parameter	Conditions	Min	Typ	Max	Unit
VIDEO OUTPUT CHARACTERISTICS					
Output Voltage Swing	AVCC − VOH, VOL − AGND		0.9	1.3	V
Output Voltage—Grounded Mode			0.06	0.150	V
Data Switching Delay: t_7[5]	VIDx = 5 V step		15.7		ns
Data Switching Delay Skew: Δt_7[5]				4	ns
INV Switching Delay: t_8[6]	VIDx = 10 V step		16.2		ns
INV Switching Delay Skew: Δt_8[6]				4	ns
Output Current			100		mA
Output Resistance			28		Ω
REFERENCE INPUTS					
VRL Range	VRH ≥ VRL	5.25		AVCC − 4	V
VRH Range	VRH ≥ VRL	VRL		VRL + 2.75	V
VRH to VRL Range[1]		0		2.75	V
VRH Input Resistance	To VRL		22		kΩ
VRL Input Current			−44		µA
VRH Input Current			111		µA
RESOLUTION	Binary Coding	12			Bits
DIGITAL INPUT CHARACTERISTICS	$T_{A\ MIN}$ to $T_{A\ MAX}$ CLK input duty cycle 40% to 60%				
CLK Frequency	DSW = HIGH			110	MHz
	DSW = LOW			85	MHz
Data Setup Time: t_1		0			ns
XFR Setup Time: t_3		0			ns
Data Hold Time: t_2		3.5			ns
XFR Hold Time: t_4		3.5			ns
CLK High Time: t_5	DSW = HIGH	2.5			ns
CLK Low Time: t_6	DSW = HIGH	3.0			ns
CLK High Time: t_7	DSW = LOW	3.5			ns
CLK Low Time: t_8	DSW = LOW	4.0			ns
C_{IN}				3	pF
I_{IH}			0.05		µA
I_{IH} TSW			333		µA
I_{IH} XFR			0.05		µA
I_{IL}			−0.6		µA
I_{IL} TSW			−1.3		µA
I_{IL} XFR			−1.2		µA
V_{IH}		2			V
V_{IL}				0.8	V
V_{TH}			1.65		V
POWER SUPPLIES					
DVCC, Operating Range		3	3.3	3.6	V
DVCC, Quiescent Current			54	70	mA
AVCC, Operating Range		11		18	V
AVCC, Quiescent Current			75	100	mA
OPERATING TEMPERATURE					
Ambient Temperature Range, T_A[7]	Still air, TSW = LOW	0		75	°C
Ambient Temperature Range, T_A[7]	200 lfm airflow, TSW = LOW	0		85	°C

[1] VDE = differential error voltage, VCME = common-mode error voltage, ΔVDE = VDE matching between outputs, ΔV = maximum deviation between outputs, and full-scale output voltage = VFS = 2 × (VRH − VRL). See the Accuracy section.
[2] Guaranteed monotonic by characterization to four sigma limits.
[3] Measured on two outputs differentially as CLK and DBx(0:11) are driven and XFR is held LOW.
[4] Measured on two outputs differentially as the others are transitioning by 5 V. Measured for both states of INV.
[5] Measured from 50% of rising CLK edge to 50% of output change. Measurement is made for both states of INV.
[6] Measured from 50% of INV transition to 50% of output change.
[7] Operation at elevated ambient temperature requires a thermally optimized PCB and additional thermal management, such as airflow across the surface of the AD8387.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltages	
AVCCx – AGNDx	18 V
DVCC – DGND	4.5 V
Input Voltages	
Maximum Digital Input Voltage	DVCC + 0.5 V
Minimum Digital Input Voltage	DGND – 0.5 V
Maximum Analog Input Voltage	AVCC + 0.5 V
Minimum Analog Input Voltage	AGND – 0.5 V
Internal Power Dissipation[1]	
TQFP E-Pad @ T_A = 25°C	4.38 W
Operating Temperature Range	0°C to 85°C
Storage Temperature Range	–65°C to +125°C
Lead Temperature Range (Soldering 10 sec)	300°C

[1] 80-lead TQFP E-Pad:
θ_{JA} = 28.5°C/W (still air) [JEDEC Standard, 4-layer PCB in still air]
θ_{JC} = 12.2°C/W
θ_{JB} = 14.6°C/W
Ψ_{JB} = 12.0°C/W
Ψ_{JT} = 0.3°C/W.

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings for extended periods may reduce device reliability.

EXPOSED PADDLE

To ensure optimized thermal performance, the exposed paddle must be thermally connected to an external plane, such as AVCC or GND, as described in the Applications section.

OVERLOAD PROTECTION

The AD8387 overload protection circuit consists of an output current limiter and a thermal switch.

When TSW is LOW, the thermal switch is disabled and the output current limiter is enabled. The maximum current at any one output is internally limited to 100 mA average. In the event of a momentary short-circuit between a video output and a power supply rail (VCC or AGND), the output current limit is sufficiently low to provide temporary protection.

When TSW is HIGH, the output current limiter, as well as the thermal switch, is enabled. The thermal switch debiases the output amplifier when the junction temperature reaches the internally set trip point. In the event of an extended short-circuit between a video output and a power supply rail, the output amplifier current continues to switch between 0 and 100 mA typical with a period determined by the thermal time constant and the hysteresis of the thermal trip point. The thermal switch, when enabled, provides long-term protection from accidental shorts during the assembly process by limiting the average junction temperature to a safe level.

MAXIMUM POWER DISSIPATION

The maximum power that the AD8387 can safely dissipate is limited by its junction temperature. The maximum safe junction temperature for plastic encapsulated devices, as determined by the glass transition temperature of the plastic, is approximately 150°C. Exceeding this limit temporarily can cause a shift in the parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 150°C for an extended period can result in device failure.

OPERATING TEMPERATURE RANGE

To ensure operation within the specified operating temperature range, it is necessary to limit the maximum power dissipation as follows.

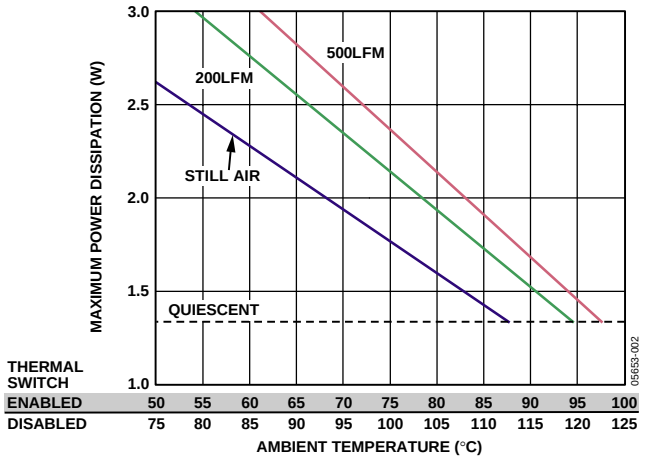


Figure 3. Maximum Power Dissipation vs. Temperature, AD8387 on a 4-Layer JEDEC PCB with Thermally Optimized Landing Pattern as Described in the Applications Section

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

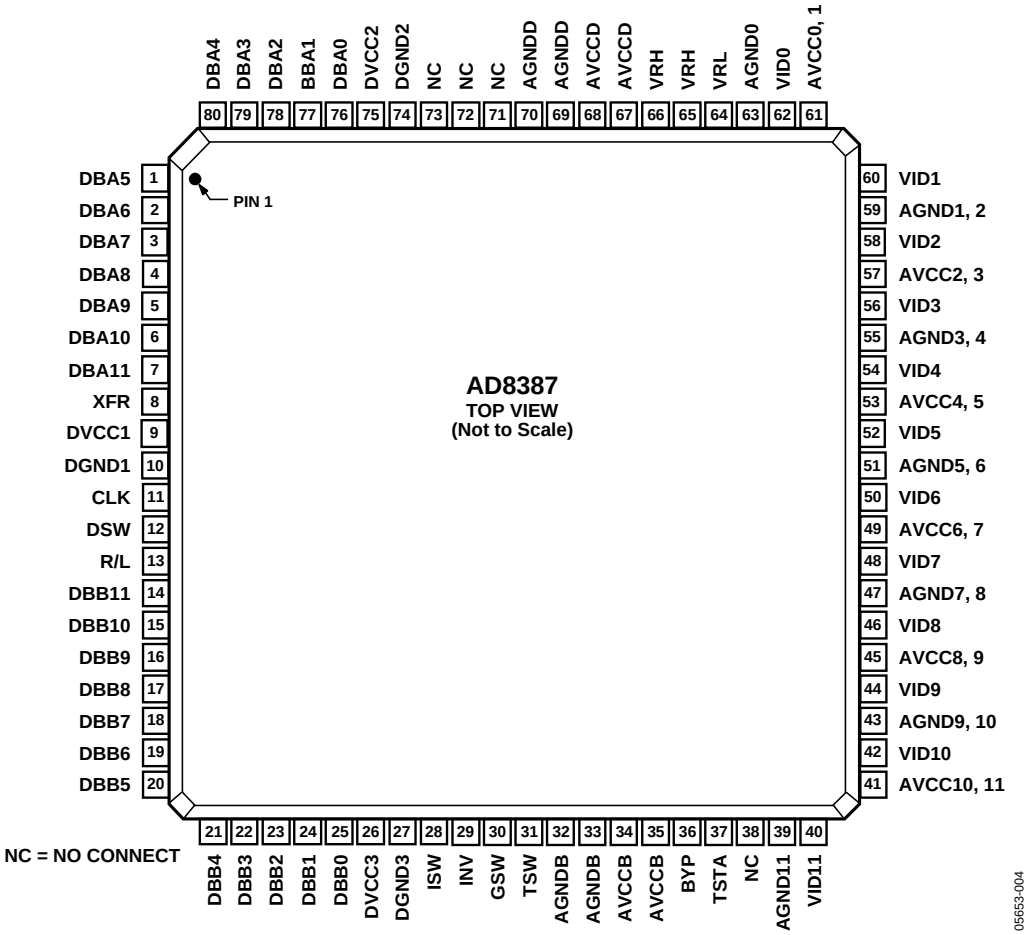


Figure 4. 80-Lead TQFP E-Pad Pin Configuration

Table 3. 80-Lead TQFP E-Pad Pin Configurations

Pin No.	Mnemonic	Function	Description
1 to 7, 76 to 80;	DBA(0:11)	Data Input	12-Bit Data Input for Even Channels. VID(0, 2, 4, 6, 8, 10), MSB = DBA11.
14 to 25	DBB(0:11)	Data Input	12-Bit Data Input for Odd Channels. VID(1, 3, 5, 7, 9, 11), MSB = DBB11.
8	XFR	Transfer/Start Sequence	Simultaneously initiates a new data loading sequence and transfers data loaded previously, to the outputs.
9, 26, 75	DVCCx	Digital Power Supplies	Digital Power Supplies.
10, 27, 74	DGNDx	Digital Ground	These pins are normally connected to the digital ground plane.
11	CLK	Clock	Clock Input.
12	DSW	Data Mode Switch	Selects Single Buss or Dual Buss Operating Modes.
13	R/L	Right/Left Select	Selects Left Direction or Right Direction Operating Mode.
28	ISW	Invert Mode Switch	Enables and Disables Column Inversion.
29	INV	Invert	Changes the Polarity of the Analog Output Signals.
30	GSW	Output Mode Switch	Enables and Disables Grounded Mode.
31	TSW	Thermal Switch	Enables and Disables Long-Term Output Protection.
32, 33, 39, 43, 47, 51, 55, 59, 63, 69, 70	AGNDx	Analog Ground	Analog Supply Returns.
34, 35, 41, 45, 49, 53, 57, 61, 67, 68	AVCCx	Analog Power Supplies	Analog Power Supplies.
36	BYP	Bypass	A 0.1 µF capacitor connected between BYP and AGND ensures optimum settling time.
37	TSTA	Test Pin	Connect This Pin to AGND.
38, 71 to 73	NC	NC	No Connect. No internal connection.
40, 42, 44, 46, 48, 50, 52, 54, 56, 58, 60, 62	VID0 to VID11	Analog Outputs	These pins are connected directly to the analog inputs of the LCD panel.
64	VRL	Video Center Reference	This Voltage Sets the Video Center Voltage. The video outputs are above this reference while INV = HIGH and below this reference while INV = LOW.
65, 66	VRH	Full-Scale Reference	Twice the voltage applied between VRH and VRL sets the full-scale video output voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

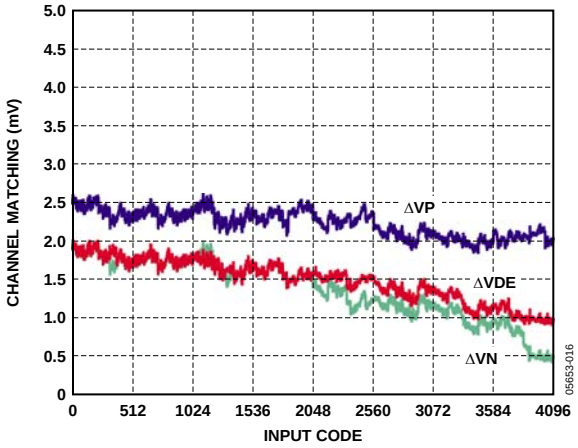


Figure 5. Channel Matching vs. Code @ T_A = 25°C

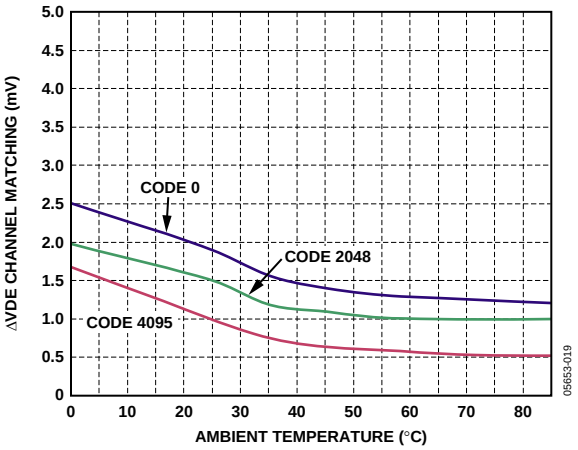


Figure 8. Channel Matching vs. T_A @ Codes 0, 2048, 4095

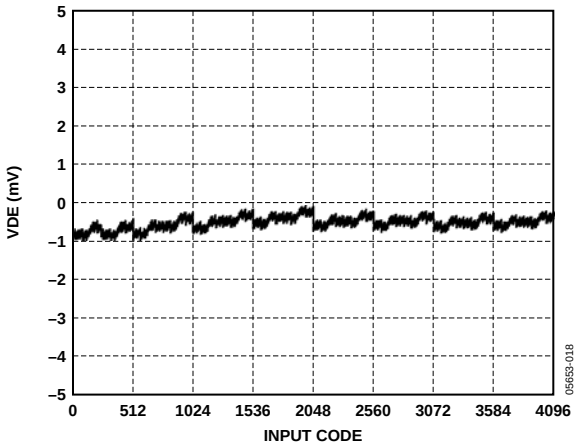


Figure 6. VDE vs. Code

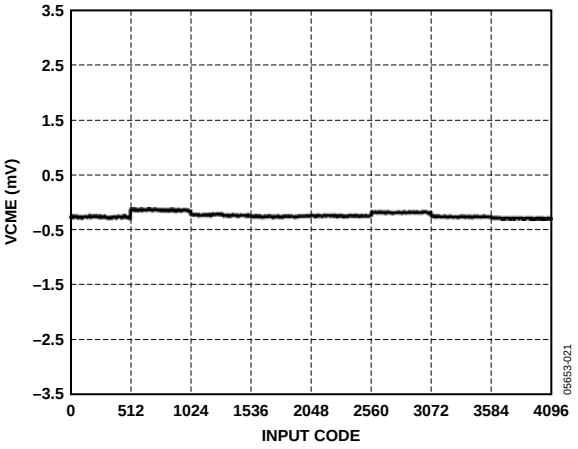


Figure 9. VCME vs. Code

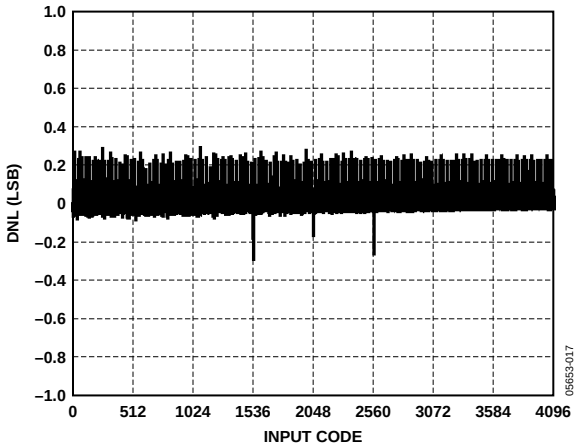


Figure 7. DNL vs. Code @ T_A = 25°C, INV = H

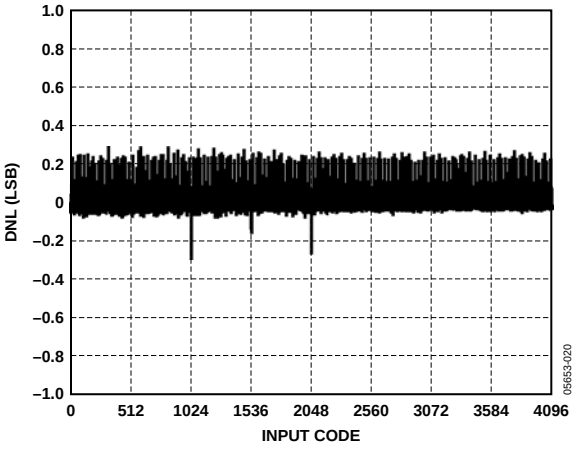


Figure 10. DNL vs. Code @ T_A = 25°C, INV = L

TIMING DIAGRAMS

SINGLE DATA BUS CONFIGURATION, DSW = LOW

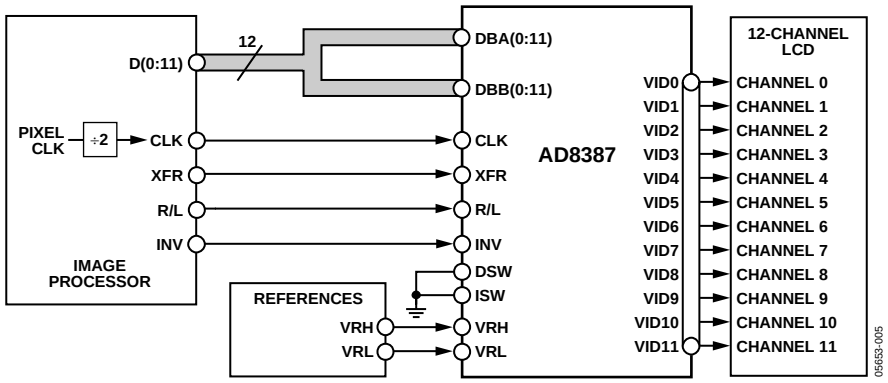


Figure 11. AD8387 in Single Data Bus System

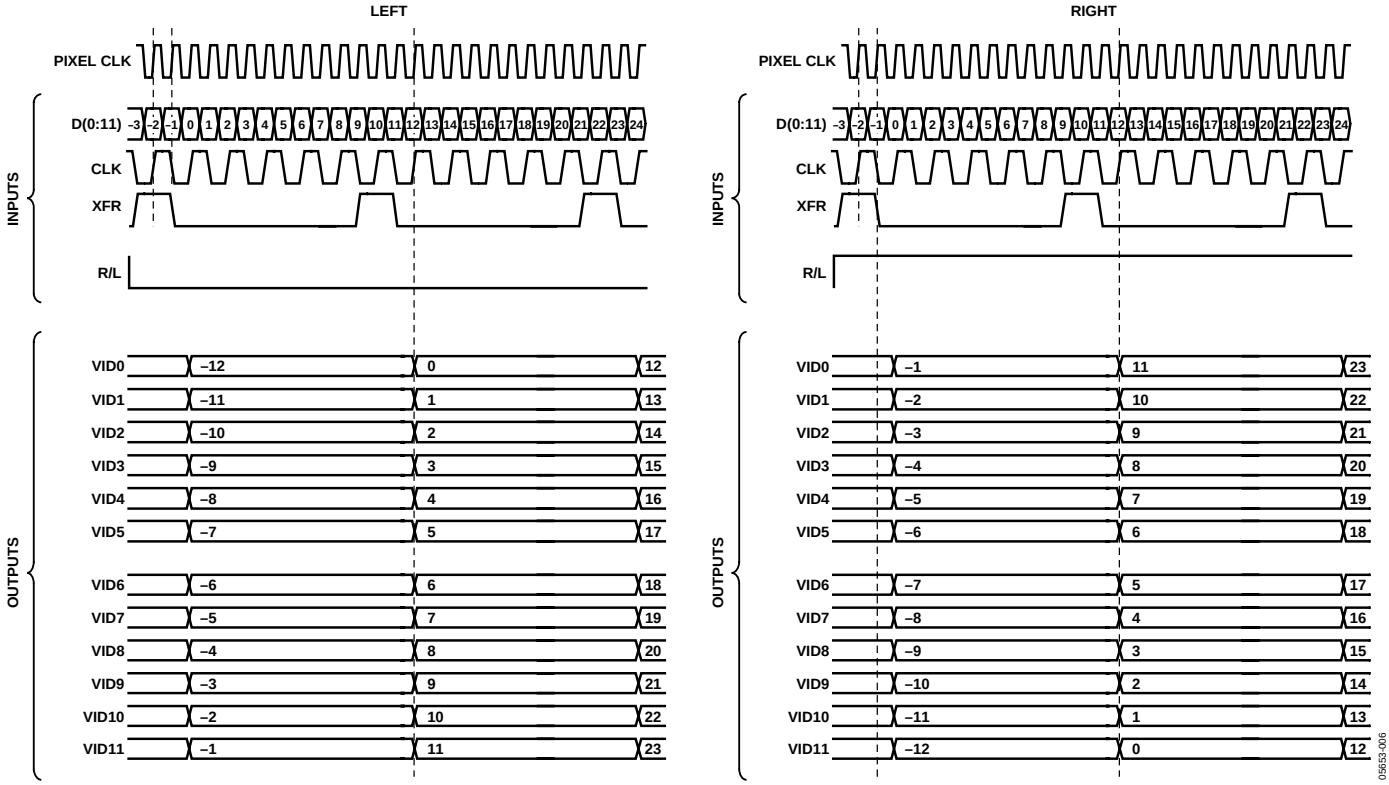


Figure 12. AD8387 in Single Data Bus Configuration Scanning Left-to-Right and Right-to-Left

DUAL DATA BUS CONFIGURATION, DSW = HIGH

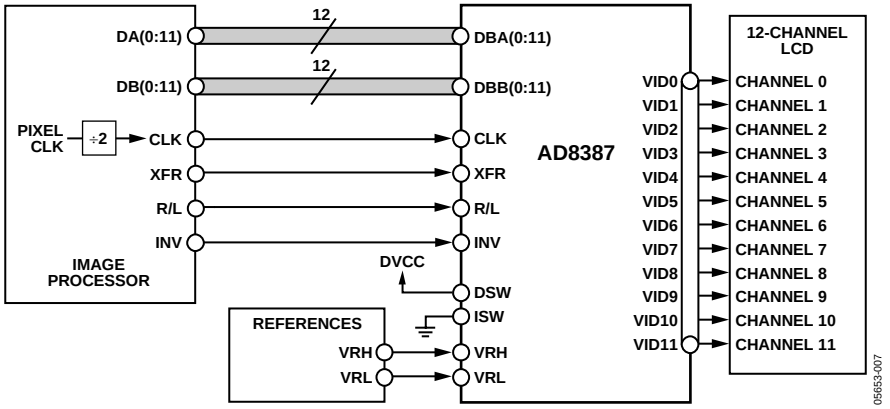


Figure 13. AD8387 in Dual Data Bus System

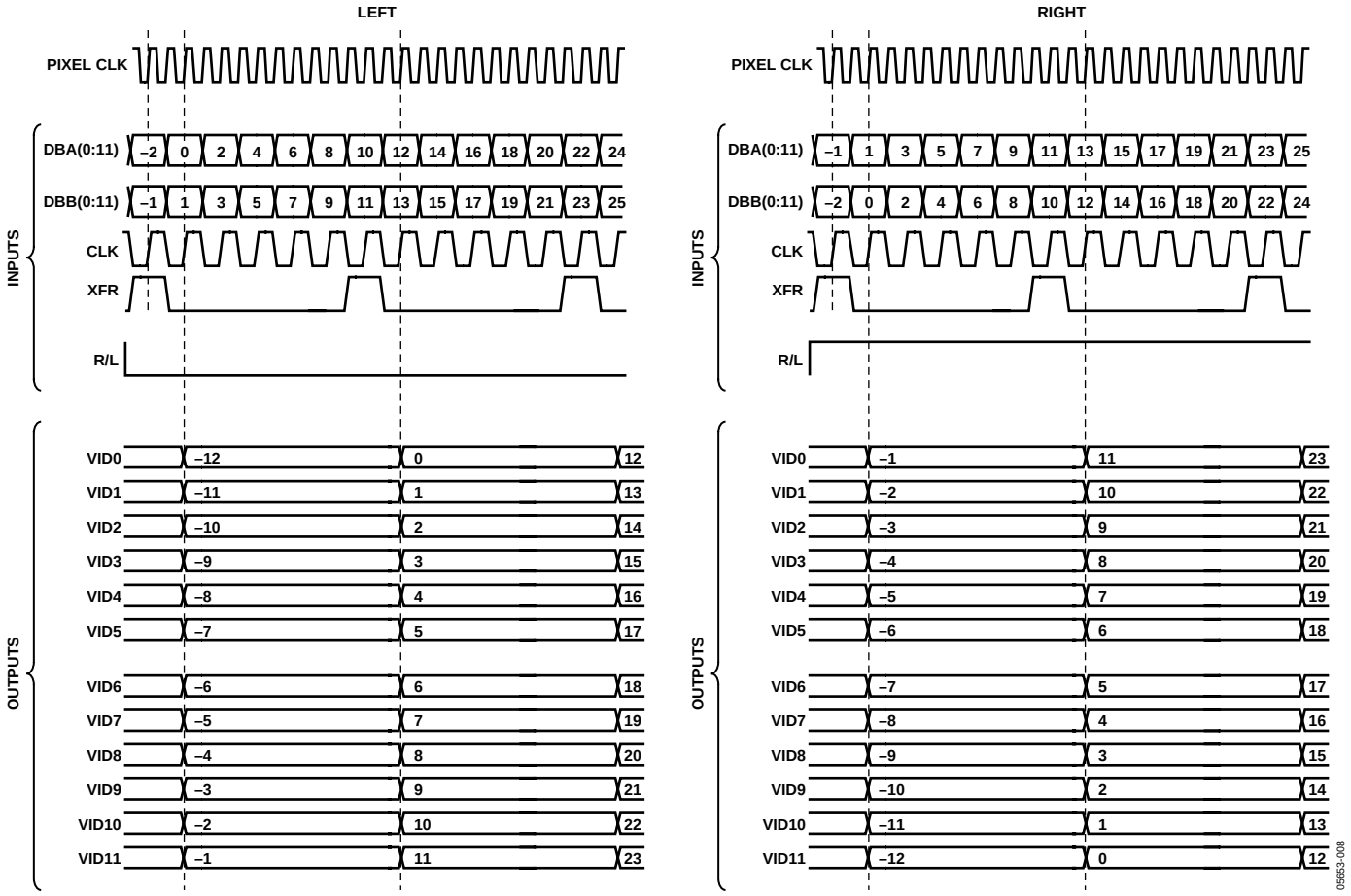


Figure 14. AD8387 in Dual Data Bus Configuration Scanning Left-to-Right and Right-to-Left

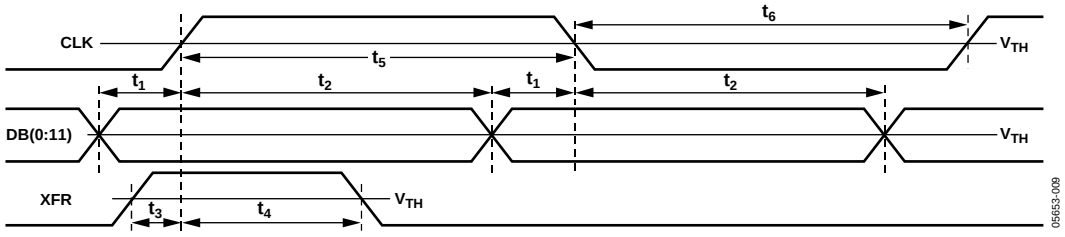


Figure 15. Input Timing (DSW = LOW)

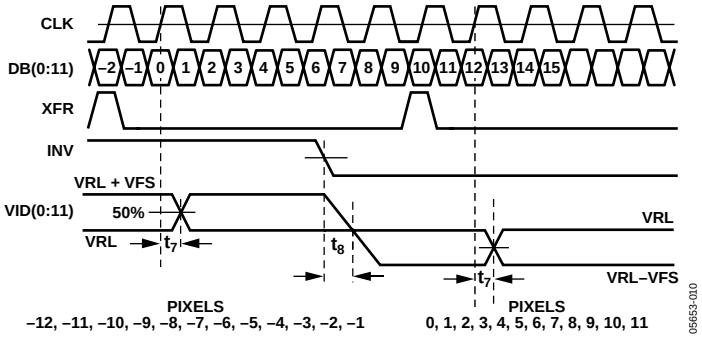


Figure 16. Output Timing (DSW = LOW)

Table 4.

Parameter	Conditions	Min	Typ	Max	Unit
Data Setup Time: t_1		0			ns
XFR Setup Time: t_3		0			ns
Data Hold Time: t_2		3.5			ns
XFR Hold Time: t_4		3.5			ns
CLK High Time: t_5	DSW = HIGH	2.5			ns
CLK Low Time: t_6	DSW = HIGH	3.0			ns
CLK High Time: t_7	DSW = LOW	3.5			ns
CLK Low Time: t_8	DSW = LOW	4.0			ns
Data Switching Delay: t_7			15.7		ns
Data Switching Delay Skew: Δt_7	VIDx = 5 V step			4	ns
Invert Switching Delay: t_8			16.2		ns
Invert Switching Delay Skew: Δt_8				4	ns

FUNCTIONAL DESCRIPTION

The AD8387 is a system building block designed to directly drive the columns of LCD microdisplays of the type popularized for use in projection systems. It has 12 channels of precision, 12-bit DACs loaded from a dual, high speed, 12-bit wide input. Precision current feedback amplifiers, providing well damped pulse response and fast voltage settling into large capacitive loads, buffer the 12 outputs. Laser trimming at the wafer level ensures low absolute output errors and tight channel-to-channel matching. Tight part-to-part matching in high resolution systems is guaranteed by the use of external voltage references.

REFERENCE AND CONTROL INPUT DESCRIPTION

Data Transfer/Start Sequence Control—Input Data Loading, Data Transfer

A valid XFR is initiated when it is held HIGH during a rising CLK edge.

Data is transferred to the outputs and a new loading sequence is initiated on the next rising CLK edge, immediately following a valid XFR.

During a loading sequence, 12-bit words are loaded sequentially into 12 internal channels.

When the AD8387 is configured for single data bus (DSW = LOW), data is loaded on both the rising and falling edges of CLK. When configured for dual data bus (DSW = HIGH), data is loaded on the rising edges of CLK only.

DSW Control—Data Mode Switch

When this input is HIGH, the AD8387 is in dual data bus mode. Data is loaded from both DBA(0:11) and DBB(0:11) on the rising CLK edge simultaneously. R/L does not change the active CLK edge in dual data bus mode. When LOW, the AD8387 is in single data bus mode. Data is loaded on the rising CLK edge from DBA(0:11) and on the falling CLK edge from DBB(0:11) when R/L is LOW. With R/L HIGH, data is loaded on the falling CLK edge from DBA(0:11) and on the rising CLK edge from DBB(0:11).

Right/Left Control—Input Data Loading

To facilitate image mirroring, the direction of the loading sequence is set by the R/L control. A new loading sequence begins at Channel 0 and proceeds to Channel 11 when the R/L control is held LOW. It begins at Channel 11 and proceeds to Channel 0 when the R/L control is held HIGH.

TSW Control—Thermal Switch Control

When this input is HIGH, the thermal switch is enabled. When LOW or left unconnected, the thermal switch is disabled.

An internal, 10 kΩ pull-down resistor disables the thermal switch when this pin is left unconnected.

GSW Control—Output Mode Switch

When this input is HIGH, the video outputs operate normally. When LOW or left open, the video outputs are forced to AGND. This function operates when AVCC power is off but requires DVCC power to be on.

INV Control and ISW Control—Analog Output Inversion

When ISW = LOW, the analog outputs' transfer function is below VRL, while INV is held LOW, and is above VRL, while INV is held HIGH.

With ISW = HIGH, the analog outputs' transfer function is above VRL for VID(0, 2, 4, 6, 8, 10) and is below VRL for VID(1, 3, 5, 7, 9, 11), while INV is held HIGH. Conversely, the analog outputs' transfer function is below VRL for VID(0, 2, 4, 6, 8, 10) and is above VRL for VID(1, 3, 5, 7, 9, 11), while INV is held LOW.

VRH, VRL Inputs—Full-Scale Video Reference Inputs

Two times the difference between VRH and VRL (analog input voltages) sets the full-scale output voltage.

$$VFS = 2 \times (VRH - VRL)$$

THEORY OF OPERATION

TRANSFER FUNCTION AND ANALOG OUTPUT VOLTAGE

The DecDriver has two regions of operation where the video output voltages are either above or below the reference voltage VRL. The transfer function defines the video output voltage as the function of the digital input code as:

$$VOUTN(n) = VIDx(n) = VRL + VFS \times (1 - n/4095), \text{ for } INV = HIGH$$

$$VOUTP(n) = VIDx(n) = VRL - VFS \times (1 - n/4095), \text{ for } INV = LOW$$

where n is the input code.

$$VFS = 2 \times (VRH - VRL)$$

A number of internal limits define the usable range of the video output voltages, VIDx, as shown in Figure 17.

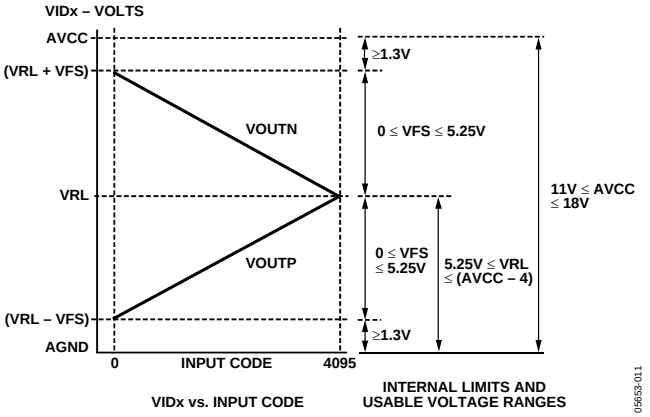


Figure 17. AD8387 Transfer Function and Usable Voltage Ranges

ACCURACY

To best correlate transfer function errors to image artifacts, the overall accuracy of the DecDriver is defined by three parameters, VDE , VCME, and ΔVDE.

VDE, the differential error voltage, measures the difference between the rms value of a channel and the ideal rms value of that channel. The defining expression is

$$VDE(n) = \frac{\left[VOUTN(n) - VOUTP(n)\right]}{2} - \left(1 - \frac{n}{4095}\right) \times VFS$$

VCME, the common-mode error voltage, measures ½ the dc bias of a channel. The defining expression is

$$VCME(n) = \frac{1}{2}\left[\frac{VOUTN(n) + VOUTP(n)}{2} - VRL\right]$$

ΔVDE measures the maximum VDE mismatch between channels. The defining equation is

$$\Delta VDE = max\{VDE(n)_{(0-11)}\} - min\{VDE(n)_{(0-11)}\}$$

ΔV measures the maximum mismatch between channels. The defining expression is

$$\Delta V(n) = max\{\Delta VN(n), \Delta VP(n)\}$$

where:

$$\Delta VN(n) = max\{VOUTN(n)_{(0-11)}\} - min\{VOUTN(n)_{(0-11)}\}$$

$$\Delta VP(n) = max\{VOUTP(n)_{(0-11)}\} - min\{VOUTP(n)_{(0-11)}\}$$

APPLICATIONS

OPTIMIZED RELIABILITY WITH THE THERMAL SWITCH

While internal current limiters provide short-term protection against temporary shorts at the outputs, the thermal switch provides protection against persistent shorts lasting for several seconds. To optimize reliability with the use of the thermal switch, the following sequence of operations is recommended.

INITIAL POWER-UP AFTER ASSEMBLY OR REPAIR

Grounded output mode is disabled, and thermal switch is enabled. Ensure that the GSW pin is HIGH and that the TSW pin is HIGH upon initial power-up and that they remain unchanged throughout this procedure.

The initial power-up sequence follows:

1. Execute the initial power-up.
2. Identify any shorts at outputs. Power down, repair shorts, and repeat the initial power-up sequence until proper system functionality is verified.
3. Disable the thermal switch.

POWER-UP DURING NORMAL OPERATION

Grounded output mode is disabled, and thermal switch is disabled.

If TSW = LOW and GSW = HIGH, all outputs go into normal operating mode with the thermal switch disabled.

POWER SUPPLY SEQUENCING

As indicated under the Absolute Maximum Ratings, the voltage at any input pin cannot exceed its supply voltage by more than 0.5 V. Power-on and power-off sequencing can be required to comply with the absolute maximum ratings.

Failure to comply with the Absolute Maximum Ratings can result in functional failure or damage to the internal ESD diodes. Damaged ESD diodes can cause temporary parametric failures, which can result in image artifacts. Damaged ESD diodes cannot provide full ESD protection, reducing reliability.

POWER-ON SEQUENCE

1. Turn on AVCC
2. Turn on VRH
3. Turn on VRL
4. Turn on DVCC
5. Disable thermal switch: TSW = LOW
6. Turn on input signals

POWER-OFF SEQUENCE

1. Turn off input signals
2. Turn off VRL
3. Turn off VRH
4. Turn off AVCC
5. Turn off DVCC

GROUNDED OUTPUT MODE DURING POWER-OFF

Certain applications require that video outputs be held near AGND during power-down. The following power-off sequence ensures that the outputs are near ground during power-off and that the Absolute Maximum Ratings are not violated.

1. Enable grounded output mode: GSW = LOW
2. Turn off input signals
3. Turn off VRL
4. Turn off VRH
5. Turn off AVCC
6. Turn off DVCC

PCB DESIGN FOR OPTIMIZED THERMAL PERFORMANCE

Although the maximum safe operating junction temperature is higher, the AD8387 is 100% tested at a junction temperature of 125°C. Consequently, the maximum guaranteed operating junction temperature is 125°C. To limit the maximum junction temperature at or below the guaranteed maximum, the package in conjunction with the PCB must effectively conduct heat away from the junction.

The AD8387 package is designed to provide enhanced thermal characteristics through the exposed die paddle on the bottom surface of the package. To take full advantage of this feature, the exposed paddle must be in direct thermal contact with the PCB, which then serves as a heat sink.

A thermally effective PCB must incorporate two thermal pads and a thermal via structure. The thermal pad on the top surface of the PCB provides a solderable contact surface on the top surface of the PCB. The thermal pad on the bottom PCB layer provides a surface in direct contact with the ambient. The thermal via structure provides a thermal path to the inner and bottom layers of the PCB to remove heat.

THERMAL PAD DESIGN

To minimize thermal performance degradation of production PCBs, the contact area between the thermal pad and the PCB should be maximized. Therefore, the size of the thermal pad on the top PCB layer should match the exposed paddle. The second thermal pad of the same size should be placed on the bottom side of the PCB. At least one thermal pad should be in direct thermal contact with an external plane, such as AVCC or GND.

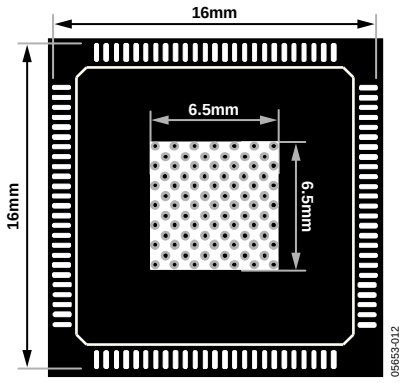


Figure 18. Land Pattern—Top Layer

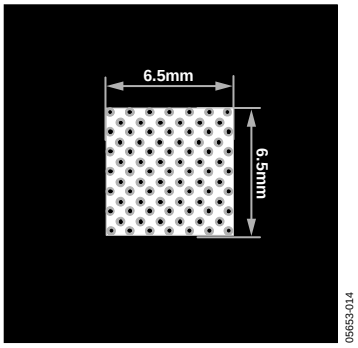


Figure 19. Land Pattern—Bottom Layer

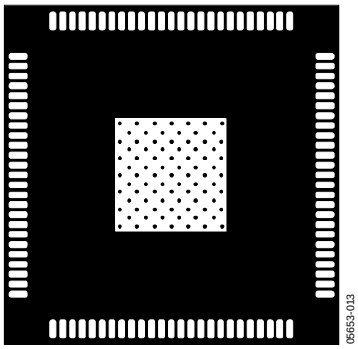


Figure 20. Solder Mask—Top Layer

THERMAL VIA STRUCTURE DESIGN

Effective heat transfer from the top to the inner and bottom layers of the PCB requires thermal vias incorporated into the thermal pad design. Thermal performance increases logarithmically with the number of vias.

Near optimum thermal performance of production PCBs is attained only when tightly spaced thermal vias are placed on the full extent of the thermal pad.

Thermal Pad and Thermal via Connections

The thermal pad on the solder side is connected to a plane. The use of thermal spokes is not recommended when connecting the thermal pads or via structure to the plane.

Solder Masking

Solder masking of the via holes on the top layer of the PCB plugs the via holes, inhibiting solder flow into the holes. To minimize the formation of solder voids due to solder flowing into the via holes (solder wicking), via diameter should be made small, and an optional solder mask can be used. To optimize the thermal pad coverage when using the solder mask, its diameter should be no more than 0.1 mm larger than the via hole diameter.

Pads are set by customer's PCB design rules.

Thermal via Holes—Circular mask, centered on the via holes. Diameter of the mask should be 0.1 mm larger than the via hole diameter.

Solder Mask—Bottom Layer

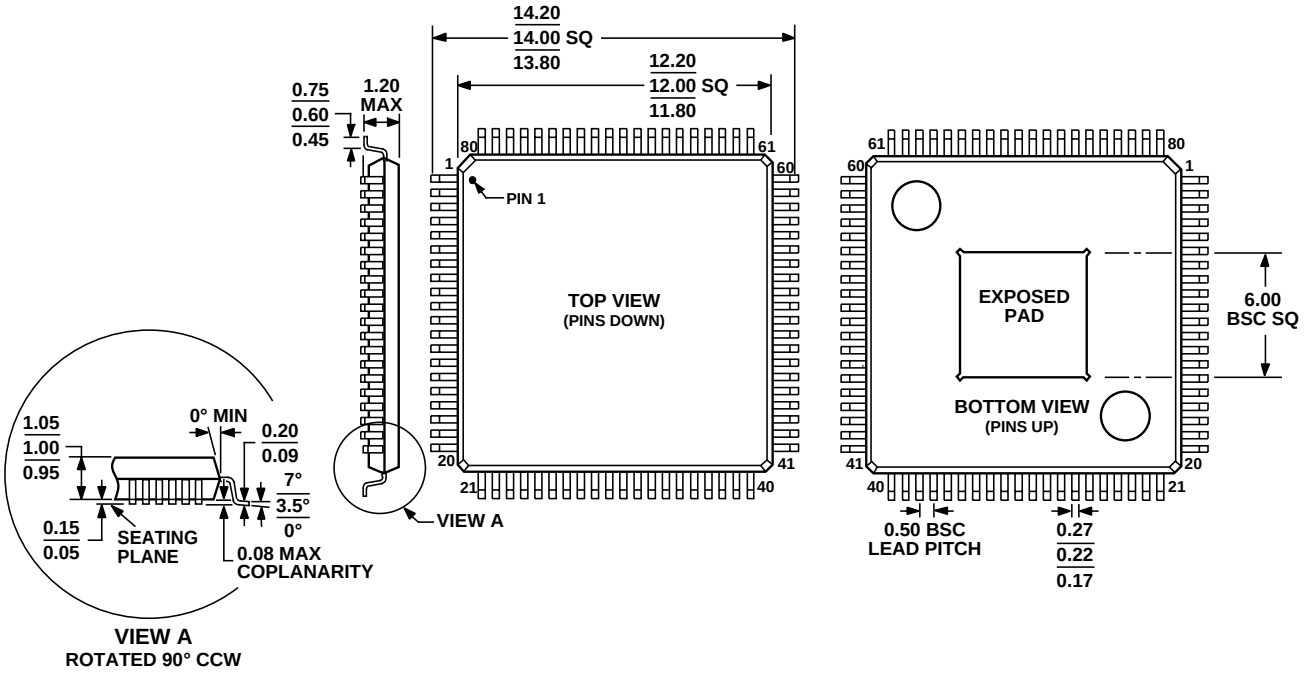
This is set by customer's PCB design rules.

AD8387 PCB DESIGN RECOMMENDATIONS

Table 5. Land Pattern Dimensions

Pad Size	Pad Pitch	Thermal Pad Size	Thermal Via Structure
0.6 mm × 0.25 mm	0.5 mm	6 mm × 6 mm	0.25 mm – 0.35 mm holes 0.5 mm – 1.0 mm grid

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-ADD-HD

Figure 21. 80-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-80-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8387JSVZ[1]	0°C to 85°C	80-Lead TQFP	SV-80-1
AD8387-EB		Evaluation Board	

[1] Z = Pb-free part.

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